Single-chip 9-band CMOS UWB Transceiver

by

Zheng Hui

A Thesis Submitted to

The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

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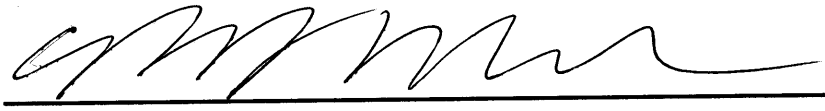

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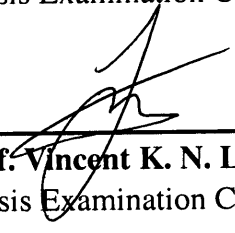

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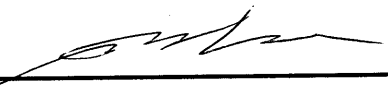

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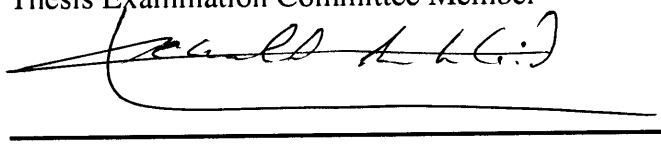

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Abstract

Driven by increasing demand of short-range and high-data-rate wireless communications, ultra-wideband (UWB) technology with target data rates up to 480Mb/s within 10-meter distance becomes more and more attractive. The UWB system utilizes the unlicensed 3.1 – 10.6 GHz frequency band with a transmit power below the FCC limit of -41.25 dBm/MHz. According to MultiBand OFDM Alliance SIG proposal, the UWB spectrum is divided into 14 bands, each with a bandwidth of 528 MHz. In this dissertation, the design and integration of a single-chip CMOS transceiver for Multi-Band OFDM (MB-OFDM) UWB system covering the first 9 frequency bands from 3.1 GHz to 8.0 GHz is presented.

Firstly, from the system point of view, dual-conversion zero-IF2 transceiver architecture is proposed. The proposed frequency scheme makes use of the upper-sideband oscillation LO1 to achieve the required image suppression without additional filtering. The system requirements of the transceiver are discussed based on which the detailed specifications of all the building blocks are derived and

verified.

Next, in terms of circuit design and implementation, a fully-integrated synthesizer is proposed employing single-sideband mixers to generate the two required LO signals. Proposed design techniques include a modified transformer-coupled quadrature VCO, a single-sideband mixer with an ultra-wideband inductive-network loading, and long-metal-line loading-insensitive layout technique. In addition, injection-locked divider techniques with different input configurations are proposed and analyzed. Specifically, a double-balanced quadrature-input quadrature-output regenerative divider and two ultra-low-voltage dividers with transformer-feedback or transformer-coupling are developed.

Design and measurements of the other building blocks in the fully-integrated transceiver, namely LNA, mixers, LPF, VGA, ADC, and DAC, will also be briefly introduced. Finally, the single-chip integration and the complete measurement results of both the receiver and the transmitter in a 0.18um CMOS process will be presented and discussed. The receiver measures maximum S11 of -13dB, maximum NF of 8.25 dB, in-band IIP3 of better than -13.7 dBm, and variable gain from 25.3 to 84.0 dB. IQ path gain and phase mismatch of the receiver chain are measured to be 0.8 dB and 4^{o} respectively. The transmitter achieves a minimum output P-1dB of -8.2 dBm, sideband rejection of better than -42.2 dBc, and LO leakage of smaller than -46.5 dBc.

Chapter 1 INTRODUCTION

1.1 Motivation

In the future, the new wireless world will be the result of a comprehensive integration of existing and future wireless systems, including wireless wide area networks (WWANs), wireless local area networks (WLANs), wireless personal area networks (WPANs); as well as home area networks that link portable devices, fixed appliances, personal computers, and entertainment equipment. In terms of communication distance, it covers all ranges from few meters to tens of kilo meters as shown in Fig. 1.1. Wireless technology will play a key role in scenarios where "everybody and everything" is connected by different types of communication links [1].

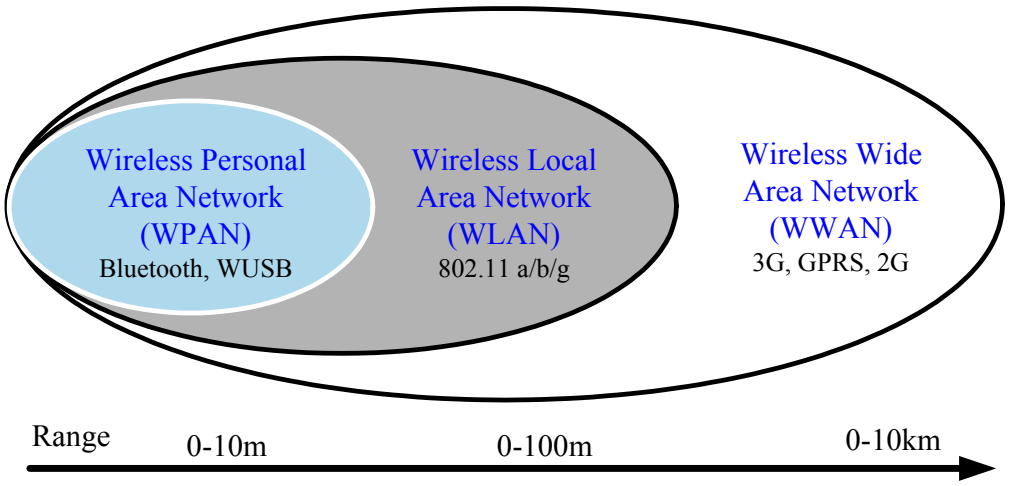

Fig. 1.1 Wireless communications coverage range

On the other hand, in today's world, most computer and consumer electronic (CE) devices still require wires to record, play or exchange data. However, the benefits of an increasingly mobile lifestyle introduced by wireless technologies in

cell phones and home PCs have resulted in greater demand for the same benefits in other consumer devices. Consumers enjoy the increased convenience of wireless connectivity. They will soon demand it for their video recording and storage devices, for real-time audio and video (AV) streaming, interactive gaming, and AV conferencing services as the need for digital media becomes more predominate in the home [2]. New wireless devices will allow people to "unwire" their lives in new and unexpected ways:

- An office worker could put a mobile PC on a desk and instantly be connected to a printer, scanner and Voice over IP (VoIP) headset.
- All the components for an entire home entertainment center could be set up and connected to each other without a single wire.
- A digital camcorder could play a just-recorded video on a friend's HDTV without anyone having to fiddle with wires.
- A portable MP3 player could stream audio to high-quality surround-sound speakers anywhere in the room.
- A mobile computer user could wirelessly connect to a digital projector in a conference room to deliver a presentation.
- Digital pictures could be transferred to a photo print kiosk for instant printing without the need of a cable.

Many technologies used in the digital home, such as digital video and audio streaming, require multiple high-throughput connections to communicate. Although, today’s wireless networking technologies developed for wirelessly connecting PCs,

such as Wi-Fi and Bluetooth Technology, are often inadequate or incapable of providing sufficiently high data rates to meet these requirements. Although data rates can reach 54 Mbps for WLAN 802.11a/g system, it still does not deliver sufficient performance to effectively allow streaming of multiple simultaneous high-quality video streams. Against this back ground, a new technology is needed to meet the needs of high-speed WPANs. The commercialization of wireless devices based on the principle of ultra-wideband (UWB) radio technology is widely anticipated.

One of the promises that UWB technology offers is the ability to provide a very high theoretical capacity. This can be seen by considering Shannon's capacity equation [3]:

$$C = B\log_2\left(1 + P/\left(NB\right)\right) \tag{1.1}$$

Where C is the Shannon capacity in bits per second, B is the bandwidth of the signal, P is the average received power, and N is the noise power spectral density. Note that, the transmit power spectral density is currently limited by the FCC rules, so the average transmit power will be $P=P_{sd}B$, where P_{sd} is the power spectral density limit allowed by the FCC. So, as the bandwidth of the UWB system increases, this equation suggests that the capacity will increase linearly with bandwidth instead of power. In [3], the capacity of a UWB system is compared with other popular, unlicensed narrowband systems also defined under the Part 15 rules; with the following transmit power for various bands:

- 16 dBm for the lower UNII band (5.15-5.25 GHz)
- 23 dBm for the middle UNII band (5.25-5.35 GHz)

- 29 dBm for the upper UNII band (5.725-5.825 GHz)
- 30 dBm (1 Watt) for the 2.4 GHz ISM band (2.4-2.284 GHz)
- -41.3 dBm/Hz for UWB signals (3.1-10.6 GHz)

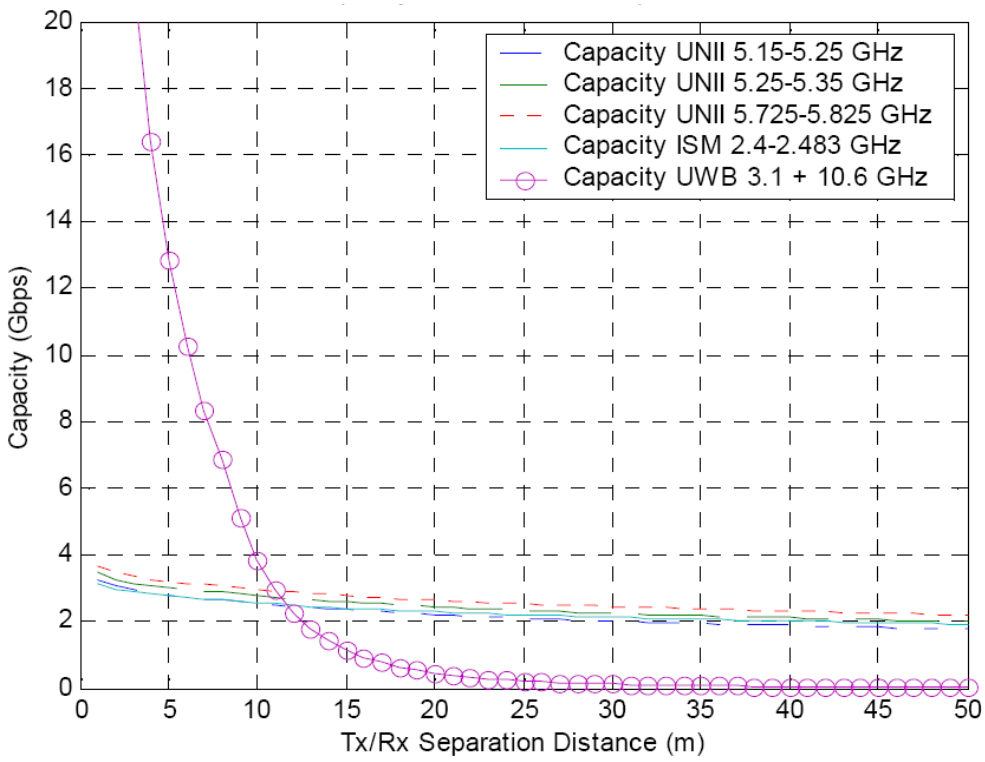

Fig. 1.2 Theoretical capacity of unlicensed systems as a function of separation distance

Fig. 1.2 clearly shows that there is a cross-over distance where the theoretical capacity is greater for UWB systems below this distance (approximately 10 meters), while the theoretical capacity is greater for the other unlicensed bands above this distance. This result suggests that, from the viewpoint of a high-throughput, short-range (less than 10 meters) wireless application requirement, UWB system is more suitable than the current unlicensed bands in the 2.4 and 5 GHz part of the spectrum.

UWB technology can enable a wide variety of WPAN applications. Examples

include:

- Replacing cables between portable multimedia CE devices, such as camcorders, and digital cameras, with wireless connectivity
- Enabling high-speed wireless universal serial bus (WUSB) connectivity for PCs and PC peripherals, including printers, scanners, and external storage devices
- Creating ad-hoc high-bit-rate wireless connectivity for CE, PC, and mobile devices

1.2 Introduction to UWB

The origins of UWB technology stem from work begun in 1962 that was generally referred to as impulse radio, baseband or carrier-free communications. The term "ultra-wideband" was first coined by the U.S. Department of Defense in 1989, and early applications leveraged the technology's properties as ground-penetrating radar [4].

A substantial change occurred in February 2002, when the FCC (2002a, b) issued a ruling that UWB could be used for data communications as well as for radar and safety applications. According to the rules set forth by the FCC on February 14, 2002, and widely accepted by the industry, ultra-wideband (UWB) devices would be required to have a –10 dB fractional bandwidth of at least 0.20 or a –10 dB bandwidth of at least 500 MHz [5]. The fractional bandwidth is defined by the expression $2(f_H - f_L)/(f_H + f_L)$, where f_H is the upper frequency and f_L is the

lower frequency at the -10 dB points. At the PHY level, FCC allocated unlicensed radio spectrum from 3.1 GHz to 10.6 GHz expressly for these purposes as shown in Fig. 1.3. The power spectral density (PSD) measured in 1-MHz bandwidth must not exceed the specified -41.25 dBm/MHz, which is equivalent to an average effective isotropic radiated power (EIRP) of 0.56 mW. The required low power is enough not to cause interference to other services operating under different rules, but sharing the same bandwidth.

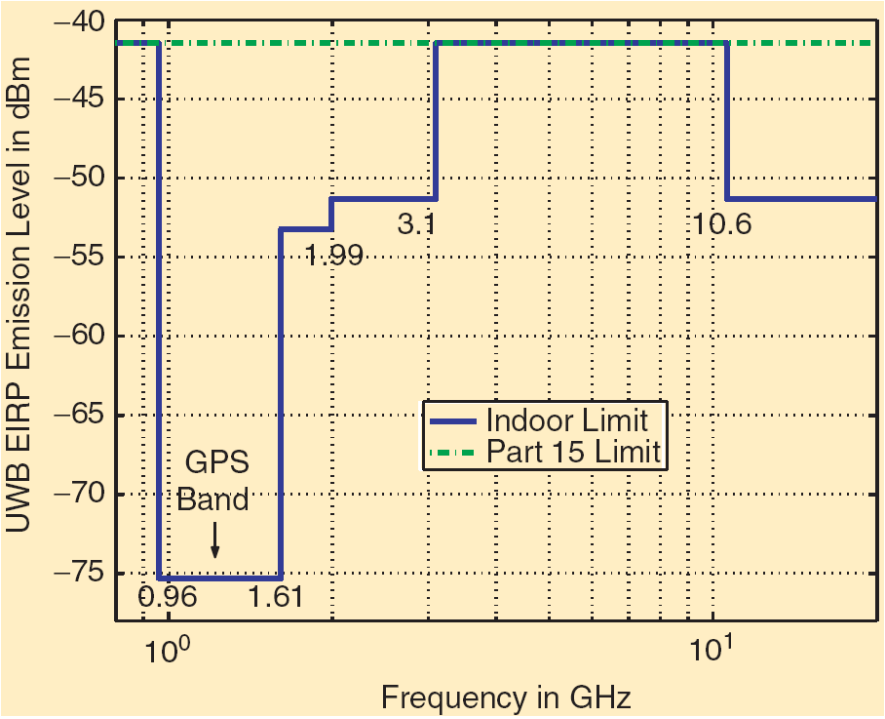

Fig. 1.3 UWB spectral mask for indoor communication systems

Up to now, the FCC does not require a UWB radio to use the entire 7.5 GHz band to transmit information, or even a substantive portion of it, but requires the adherence to the specified spectral mask. The flexibility provided by the FCC ruling greatly expands the design options for UWB communication systems. Designers are free to use a combination of sub-bands within the spectrum to optimize system

performance, power consumption and design complexity. Given this option for a multi-band system, information can either be transmitted by the traditional pulse-based single carrier method (Impulse Radio Approach) or by more advanced multi-carrier techniques (Multibanded Approach).

1.2.1 Impulse Radio Approach

Impulse radio is the technology most often associated with UWB. As shown in Fig. 1.4, a very short pulse in the time domain, typically in the order of a nanosecond, can generate a signal that is spread across a wide spectrum in the frequency domain. A UWB system can be designed to use the 7500 MHz available UWB spectrum with impulse radio approach. To realize it, the signal can be shaped so that its envelope occupies the full spectrum or part of the UWB spectrum.

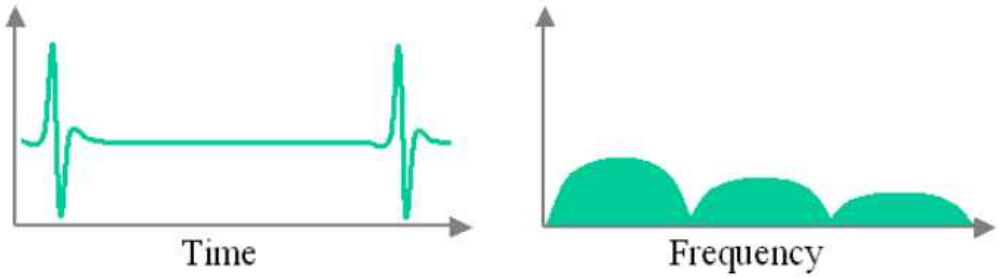

Fig. 1.4 Ultra-wideband impulse radios

Information can be encoded in a UWB signal in a variety of methods. The most popular modulation schemes developed to date for UWB are pulse-position modulation (PPM), pulse-amplitude modulation (PAM), on-off keying (OOK), and binary phase-shift keying (BPSK) [6].

- PPM

PPM is based on the principle of encoding information with two or more

positions in time, which is referred to the nominal pulse position, as shown in Fig. 1.5. A pulse transmitted at the nominal position represents a 0, and a pulse transmitted after the nominal position represents a 1.

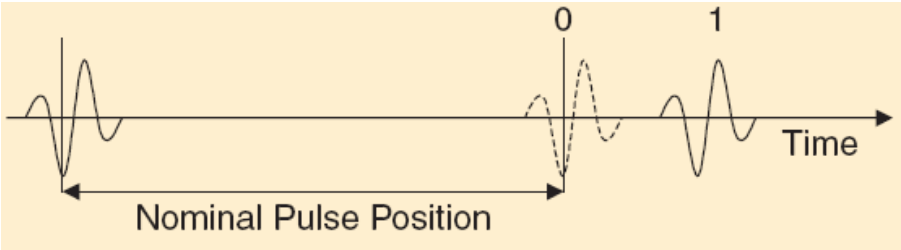

Fig. 1.5 PPM Modulation

● PAM

PAM is based on the principle of encoding information with the amplitude of the impulses, as shown in Fig. 1.6. The picture shows a two-level modulation, for zero and lower amplitude respectively, where one bit is encoded in one impulse.

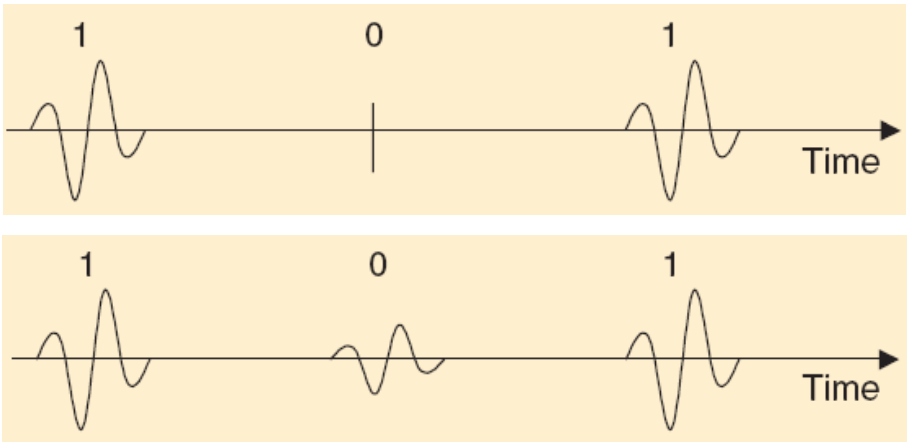

Fig. 1.6 PAM Modulations

● BPSK (Biphase)

In biphase modulation, information in encoded with the polarity of the impulse, as shown in Fig. 1.7. The polarity of the impulses is switched to encode a 0 or a 1. In this case, only one bit per impulse can be encoded because there are only two polarities available to choose from.

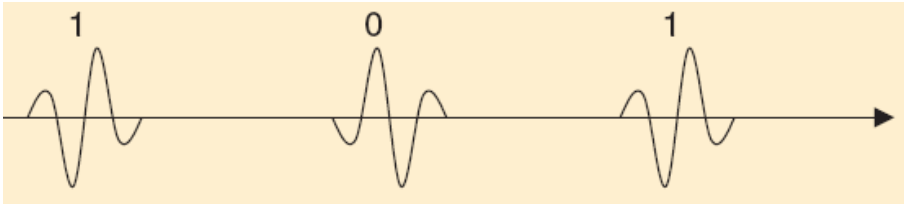

Fig. 1.7 Biphase Modulation

However, the impulse radio approach faces the very important challenges of coexisting with existing narrowband systems. Most companies would prefer not to have a UWB signal occupying their frequency band, particularly those companies involved with critical services like GPS [7]. To successfully coexist, notch filters might be required in impulse radio to mitigate the effects of narrowband interferers. However, they are not an ideal solution because they either increase the receiver's noise figure ore require higher performance LNAs. Another problem with the notch filter is that they are not adaptive and need to be realized with off-chip dedicated hardware. In addition, notch filters, in most cases, will distort the received signals.

The short duration of the pulses of impulse radio presents several technical challenges as well [7]. Generation of such an impulse type of signal which spans multiple Giga-Hertz bandwidth to efficiently fit into the FCC's spectral mask is challenging. Their short duration makes them more susceptible to timing jitter. In terms of scaling the design to higher data rates, some of the options available with an impulse based system are to increase the pulse repetition frequency, use higher-order modulation, or use spread spectrum technology. The first option would make the system more vulnerable to inter-symbol interference (ISI). The second would increase the peak-to-average power ratio and impose greater linearity requirements on the circuits. The last option requires careful selection of the properties of the

codes. The challenges facing impulse radio have made people look towards a multibanded approach to UWB.

1.2.2 Multibanded Approach

A more recent approach to UWB is a multiband system where the UWB frequency band from 3.1 GHz to 10.6 GHz is divided into several smaller bands. Each of these bands has a bandwidth greater than 500 MHz, to comply with the FCC definition of UWB. Several schemes based on multibands have been proposed.

On the first case, the pulse signal can be shaped so that it occupies only 500 MHz bandwidth, allowing 15 such signals to cover the entire band. The pulsed multicarrier UWB system is similar to an OFDM signal; the individual pulses can be systematically generated by generating different "carrier" frequencies as needed and modulating them with a common baseband pulse that has an approximate 500 MHz bandwidth.

Multiband UWB system on the one hand can avoid transmitting on the frequency bands where other wireless systems like 802.11a are presented by not using those frequency bands. This approach on the other hand, has the additional benefit of being able to adapt to the different regulatory requirements of various countries by employing different sets of sub-bands. Compared with impulse radio, in multiband UWB, the pulses are not as short. So the pulse repetition frequency can be lower than that of the impulse radio at the same peak power, diminishing the effects of ISI and timing jitter [7]. This approach also eases the requirements of pulse shaping filters and avoids having to use notch filters. Also, scaling the data rates can

be achieved by varying the number of carriers employed in the system.

In the second case, in addition to the pulsed multiband UWB system, orthogonal frequency division multiplexing (OFDM) has been proposed as the modulation method for the multiband UWB system. The Multiband OFDM (MB-OFDM) Alliance (MBOA) was formed in June 2003 to support an UWB specification based on OFDM. In fact, based on broad industry support and the strong technical attributes of MB-OFDM, WiMedia Alliance in May 2004 has endorsed MBOA's specifications for use with the WiMedia Convergence Platform. In the next section, an overview of MB-OFDM specifications proposed by MBOA will be presented.

1.2.3 MB-OFDM Overview

It is notable that the OFDM modulation technique is a very powerful technology, which has been successfully applied to several other high-performance, popular commercial communications systems including Wi-Fi 802.11a/g, WiMAX 802.16a, and the global ADSL standards. MB-OFDM technology allows good performance in a multi-path environment, and immunity to narrowband interference, as well as allows shaping of the spectrum to avoid introducing interference by eliminating specific carriers, and is spectrally efficient.

According to the MBOA proposal [8], the UWB spectrum is divided into 14 bands, each with a bandwidth of 528 MHz. The first 12 bands are then grouped into 4 band groups consisting of 3 bands each, and the last two bands are grouped into a fifth band group, as shown in Fig. 1.8.

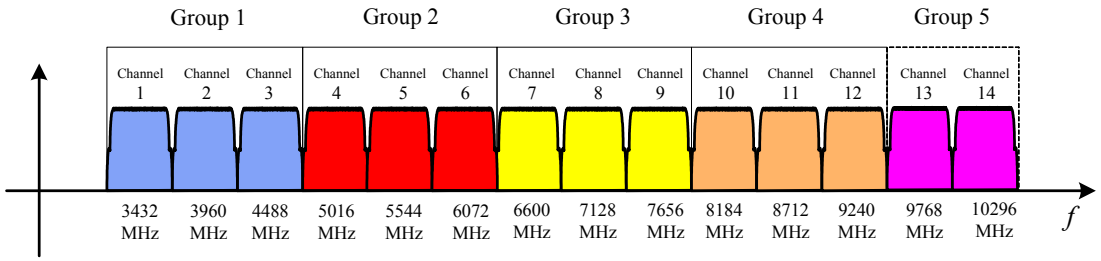

Fig. 1.8 Band groups allocation

Support for the first band group (lowest three frequency bands) shall be mandatory. The other four groups are reserved for future use or for high performance operation. The relationship between center frequency and band number is given by the following equation: Band center frequency = 2904 + 528×nb, nb =1…14 (MHz). The band allocation is summarized in Table 1.1.

Table 1.1 Summary of the bands allocation

BAND_ID (*nb*)	**Lower Frequency (*fl*)**	**Center Frequency (*fc*)**	**Upper Frequency (*fh*)**	**BAND_ID (*nb*)**	**Lower Frequency (*fl*)**	**Center Frequency (*fc*)**	**Upper Frequency (*fh*)**
1	**3168 MHz**	**3432 MHz**	**3696 MHz**	**8**	**6864 MHz**	**7128 MHz**	**7392 MHz**
2	**3696 MHz**	**3960 MHz**	**4224 MHz**	**9**	**7392 MHz**	**7656 MHz**	**7920 MHz**
3	**4224 MHz**	**4488 MHz**	**4752 MHz**	**10**	**7920 MHz**	**8184 MHz**	**8448 MHz**
4	**4752 MHz**	**5016 MHz**	**5280 MHz**	**11**	**8448 MHz**	**8712 MHz**	**8976 MHz**
5	**5280 MHz**	**5544 MHz**	**5808 MHz**	**12**	**8976 MHz**	**9240 MHz**	**9504 MHz**
6	**5808 MHz**	**6072 MHz**	**6336 MHz**	**13**	**9504 MHz**	**9768 MHz**	**10032 MHz**
7	**6336 MHz**	**6600 MHz**	**6864 MHz**	**14**	**10032 MHz**	**10296 MHz**	**10560 MHz**

The UWB system provides a wireless PAN with data payload communication capabilities of 53.3, 80, 106.7, 160, 200, 320, 400, and 480 Mb/s. The support of transmitting and receiving at data rates of 53.3, 106.7, and 200 Mb/s shall be

mandatory.

This standard specifies a Multiband Orthogonal Frequency Division Modulation (MB-OFDM) scheme to transmit information. A total of 128 sub-carriers are defined, and 122 sub-carriers per band are used to transmit the information, including 100 data carriers as shown in Fig. 1.9. Wherein, twelve of the subcarriers are dedicated to pilot signals in order to make coherent detection robust against frequency offsets and phase noise. These pilot signals shall be put in subcarriers numbered –55, –45, –35, –25, –15 –5, 5, 15, 25, 35, 45, and 55. In addition, ten of the subcarriers at the edges of the occupied frequency band shall be termed guard subcarriers. Implementations may exploit the guard subcarriers for various purposes, including relaxing the specs on transmit and receive filters as well as possible performance improvements.

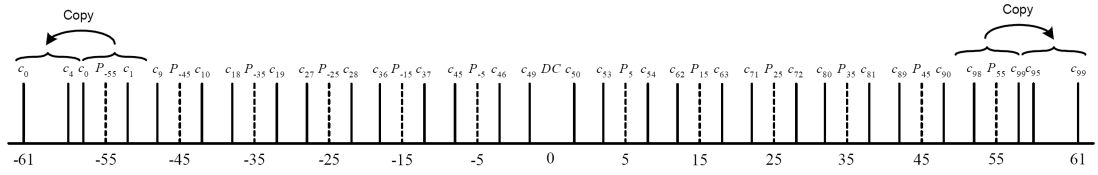

Fig. 1.9 Sub-carriers allocation

To avoid difficulties in DAC and ADC offsets and carrier feed-through in the RF system, the sub-carrier falling at DC (0th sub-carrier) is not used. Frequency-domain spreading, time-domain spreading, and forward error correction coding are used to vary the data rate. The coded data is then spread using a time-frequency code (TPC). This standard specifies two types of time-frequency codes (TFCs): one where the coded information is interleaved over three bands, referred to as Time-Frequency Interleaving (TFI); and, one where the coded information is transmitted on a single band, referred to as Fixed Frequency Interleaving (FFI). Support for both TFI and

FFI shall be mandatory. Moreover, for data rates 200 Mb/s and lower, the binary data shall be mapped onto a QPSK constellation. Whereas, for data rates 320 Mb/s and higher, the binary data shall be mapped onto a multi-dimensional constellation using a dual-carrier modulation (DCM) technique.

The TX and RX architecture for a multiband OFDM system are very similar to that of a conventional wireless OFDM system. The main difference is that the multiband OFDM system uses a time-frequency kernel to specify the center frequency for the transmission of each OFDM symbol. Fig. 1.10 shows one realization of a time-frequency code, where the first OFDM symbol is transmitted on sub-band 1, the second OFDM symbol is transmitted on sub-band 3, the third OFDM symbol is transmitted on sub-band 2, the fourth OFDM symbol is transmitted on sub-band 1, and so on. As shown in Fig.1.10, a guard interval (9.5 ns) is appended to each OFDM symbol. So that, the switching time between band frequencies can not exceed 9.5 ns.

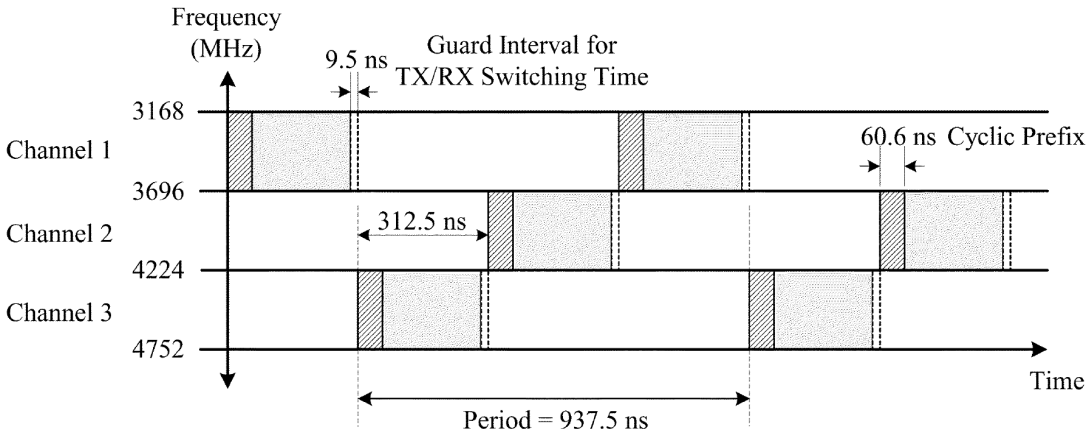

Fig. 1.10 Example of time-frequency coding for 3 bands

Table 1.2 summarizes the timing-related parameters.

Table 1.2 Timing-related parameters

Parameter	Description	Value
f_s	Sampling frequency	528 MHz
N_{FFT}	Total number of subcarriers (FFT size)	128
N_D	Number of data subcarriers	100
N_P	Number of pilot subcarriers	12
N_G	Number of guard subcarriers	10
N_T	Total number of subcarriers used	122 (= N_D + N_P + N_G)
Δ_f	Subcarrier frequency spacing	4.125 MHz (= f_s / N_{FFT})
T_{FFT}	IFFT and FFT period	242.42 ns (Δ_f^{-1})
N_{ZPS}	Number of samples in zero-padded suffix	37
T_{ZPS}	Zero-padded suffix duration in time	70.08 ns (= N_{ZPS} / f_s)
T_{SYM}	Symbol interval	312.5 ns (= T_{FFT} + T_{ZPS})
F_{SYM}	Symbol rate	3.2 MHz (= T_{SYM}^{-1})
N_{SYM}	Total number of samples per symbol	165 (= N_{FFT} + N_{ZPS})

1.3 Challenges and Our Objective

UWB offers great promise and potential, but at the same time poses even greater challenges. Since many applications enabled by UWB technology are expected to be in handheld devices, low cost and low power consumption is expected. Today, voltage levels available in CMOS are getting lower with technology scaling in order to provide faster speeds according to Moore's Law, while, the low transmit power of UWB emissions allows for the possibility of greater integration of the baseband and RF circuits into lower cost CMOS process without external power amplifier.

In this dissertation, the objective is on the design and integration of the MB-OFDM UWB RF transceiver including IQ ADCs and DACs in low-cost 0.18-μm CMOS process, which occupies the frequency from 3.1 GHz to 8.0 GHz

with 9 bands.

1.4 Outline of The Dissertation

The dissertation is organized as follows.

Chapter 2 discusses the transceiver system architectures and specifications. Different potential architectures for 9-band UWB transceiver system are addressed; their advantage and disadvantage are compared. A dual-conversion zero-IF architecture with upper-sideband oscillation LO1 is then proposed. The receiver and transmitter specifications are described. Building blocks specifications are then derived from system specifications.

Chapter 3 presents the design and integration of the proposed fast-band-switching frequency synthesizer for 9-band UWB systems. Each block in the synthesizer, including phase-locked loop, quadrature VCO, high-frequency multiplexer, and wideband single-sideband mixer are discussed in great detail. A wideband inductive-network loading, a modified transformer-coupled quadrature VCO and long-metal-line loading-insensitive layout technique are proposed. Finally, the measurement results are shown.

Chapter 4 describes different types of high-frequency divider design. This chapter begins with a brief discussion of the conventional injection-locked divider. More advanced injection-locked dividers with different input configurations are analyzed and studied. A double-balanced quadrature-input quadrature-output regenerative (QIQO) divider is proposed, which provides a mechanism to achieve an

output IQ phase sequence that is inherently tracked with the input IQ phase sequence. Two ultra-low-voltage (ULV) dividers with transformer-feedback or transformer-coupling are proposed and analyzed, which can operate at low-supply that is comparable to the device threshold voltage. In addition, a dual-loop regenerative model is proposed and used to analyze all the dividers. The analyses of output IQ phase sequence and input frequency range of the divider are emphasized.

Chapter 5 presents the design of the high-speed DAC for UWB transmitter. Two 6-bit current-steering IQ DACs with sampling clock frequency up to 1 GHz are proposed. Some critical building design, such as current cell and latch, are described. Layout design issues and considerations on high-speed operation and good-matching requirement are addressed. The measurement results are given.

Chapter 6 introduces the design of the other building blocks in the UWB transceiver. That contains LNA, down-mixer, channel-selection-filter, VGA and ADC in the receiver, low-pass-filter, up-mixer and output buffer in the transmitter. The schematic, design consideration and measurement results are presented.

Chapter 7 presents the integration and measurement of the whole UWB transceiver. The layout floor-plan and encountered problems during transceiver integration are discussed. The testing method and set-up for receiver and transmitter are described. Completed measurement results on receiver and transmitter are presented.

Chapter 8 draws the final conclusions.

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Chapter 2 SYSTEM ARCHITECTURE AND SPECIFICATION

2.1 Overview

To realize our single-chip fully-integrated 9-band UWB transceiver, the suitable system architecture and required specifications both for system and build blocks have to be studied carefully. In this chapter, the transceiver system architectures and specifications are first explored. Different potential architectures for our 9-band UWB transceiver system are addressed; their advantages and disadvantages are compared. On top of that, a dual-conversion zero-IF architecture with upper-sideband oscillation LO1 is then proposed. Consequently, the receiver and transmitter specifications are described. Finally, the building blocks specifications are then derived from the system specifications.

2.2 Transceiver Architectures

In today's world of miniaturization, there is an increasing industry pressure to reduce the cost of communication chips. This pressure has driven designers to develop a single-chip CMOS wireless transceiver. This single-chip integration is particularly attractive for its potential in achieving the highest possible level of integration and the best performance in terms of cost, size, and power consumption. To facilitate the single-chip implementation with minimum cost and power, the receiver and transmitter designs are done simultaneously. Consequently, various

transceiver topologies have been considered including direct conversion, dual conversion, low IF and zero IF, each having advantages and disadvantages [1].

2.2.1 Direct-Conversion Zero-IF Architecture

The motivation of eliminating off-chip components has led to the zero-IF architecture, as shown in Fig. 2.1. It is a direct-conversion (zero-IF) transceiver for direct-sequence spread spectrum systems that include frequency synthesizer, received signal strength indicator (RSSI) and on-chip filtering.

In the receiver, the entire RF spectrum is down-converted to DC directly using a single-stage mixer with the LO frequency which is equal to the input carrier frequency. An IQ down-conversion mixer is needed to translate and to generate in-phase and quadrature-phase (I and Q) signals for further signal processing. A high roll-off low-pass filter (LPF) is used to perform the channel selection. In addition, all of the RF channels are frequency translated to baseband before any channel filtering is performed. This allows the possibility of on-chip programmable filter structures to accommodate the variable channel bandwidth in turn facilitating multi-mode or multi-standard operation.

Similar to the receiver, the transmitter modulates and up-converts the baseband signal in one step with an IQ up-conversion mixer. Where, the image rejection is done actively with the combination of the IQ baseband signals and the IQ LO signals.

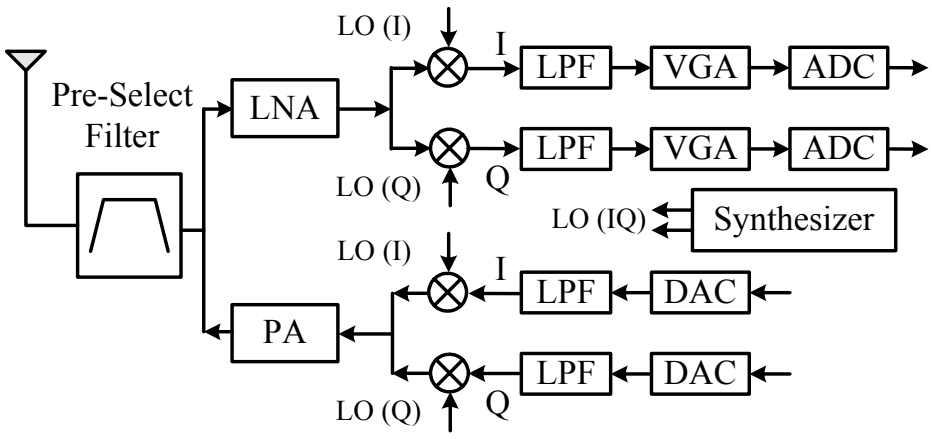

Fig. 2.1 Direct-conversion zero-IF transceiver architecture

As a significant advantage, this architecture eliminates the need for any image-rejection filters both at receiver and transmitter chains as there are no image signals created by a single step frequency translation, which offers a high level of integration. Overall, the direct-conversion zero-IF architecture is excellent at saving cost, die area and power consumption. However, there are problems associated with this architecture. First of all, because the local oscillator is at the same frequency as the RF carrier, the potential exists for LO leakage to either the mixer input or to the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect off nearby objects and be "re-received' consequently self-mixing with the local oscillator resulting in a time-varying or "wandering" DC offset at the output of the mixer [2]. This time varying DC offset, together with inherent baseband circuit offsets as well as DC components arising from second order intermodulation and I/f noise, significantly reduces the dynamic range of the receiver. In addition, a direct conversion receiver requires a high-frequency, low phase-noise, channel-select frequency synthesizer, which is difficult to achieve with a relatively low-Q integrated VCO.

Another barrier to implement a direct-conversion zero-IF architecture is LO or VCO pulling. LO pulling is a phenomenon in which the LO frequency is controlled by a strong PA signal if both the output and oscillator are at the same high frequency. Without exceptional isolation between the PA and VCO, integration of the PA with the VCO in a single-step transceiver may be difficult to achieve.

Indeed, to deal with the problem with image rejection, many UWB transceivers focus on the direct-conversion zero-IF transceiver architecture [3]-[5]. However, in addition to the aforementioned problems, this UWB transceiver architecture has to deal with a wideband and high frequency IQ LO requirement. As the number of frequency bands increased up to 9 to cover from 3.1 GHz to 8.0 GHz for UWB systems, it becomes the most challenge requirement to generate such wideband and high frequency IQ LO signals, in particular in low-cost CMOS technology. The possibility to generate the desired LO signals for UWB systems have been demonstrated. As illustrated in [6], two Single Side-band (SSB) mixers can be used to generate the IQ output. However, the phase accuracy largely depends on the quadrature input signals of the SSB-Mixers, which is not quite reliable especially at such high frequency. The divided-by-2 solution can guarantee high phase accuracy [4], but that requires operation at double frequency and larger power.

2.2.2 Direct-Conversion Low-IF Architecture

Another architecture which alleviates many of the DC offset and LO pulling problems that plague direct conversion transceivers is the Low-IF architecture. In this architecture, the LO frequency is offset from the input carrier frequency. Similar

to zero-IF, a single mixer stage is used to frequency translate all of the desired channels to a low-IF frequency in the receiver; this IF is typically in the order of one or two channel bandwidths. The primary advantage of a low-IF system is that the desired channel is offset from DC. Therefore, the typical problems arising from DC offsets found in zero-IF transceivers may be bypassed.

On the other hand, in Low-IF transceivers some methods of image-rejection must be performed because the desired carrier is down-converted to a low-IF. This is accomplished by using some variant of an image-rejection mixer. Because the IF is in the order of the channel bandwidth, all of the image band attenuation must be performed by an on-chip image-rejection mixer where the image rejection is limited by matching considerations to about 40dB [2]. In addition, it is not a suitable choice for wideband transceivers. Unlike narrow-band transceivers, wideband transceivers have more critical problems with image rejection because the images lie within the signal bandwidth and can only be effectively rejected with high attenuation tracking RF filters. Moreover, the baseband is required to operate at higher frequency with higher power compared with that of the zero-IF architecture.

2.2.3 Dual-Conversion Low-IF Architecture

The problems mentioned above for the direct-conversion low-IF architecture can be alleviated by using a dual-conversion low-IF architecture. A popular dual-conversion receiver architecture that eliminates a need of an RF tracking image-rejection filter is to first up-convert the desired signals to a very high and fixed IF frequency so that an off-chip RF filter can be employed to reject the image

and then to down-convert it to a low-IF with a fixed LO2 frequency [7]. One example is shown in Fig. 2.2, a wideband receiver for Cable-TV tuner systems [8]. The broad-band input first enters an up-converter which translates the desired channel to a 1.22-GHz IF to place the image of the desired channel far away, while reducing the number of spurs falling at the IF band. After up-conversion and IF filtering, a down-conversion mixer converts the 1.22-GHz signal down to a second low-IF frequency using a fixed second LO2. A second off-chip (or on-chip) IF filter provides additional channel selection. The dual-conversion frequency plan drastically reduces in-band spurious products while placing the image frequency far from the desired channel. However, the main challenges are not only with off-chip high-Q RF filter and LO1 with an extremely wide frequency tuning range but also with high circuit complexity and high power consumption. The circuit complexity and power can be significantly reduced by replacing the first up-conversion mixer to a down-conversion mixer at a cost of much more stringent image rejection requirement.

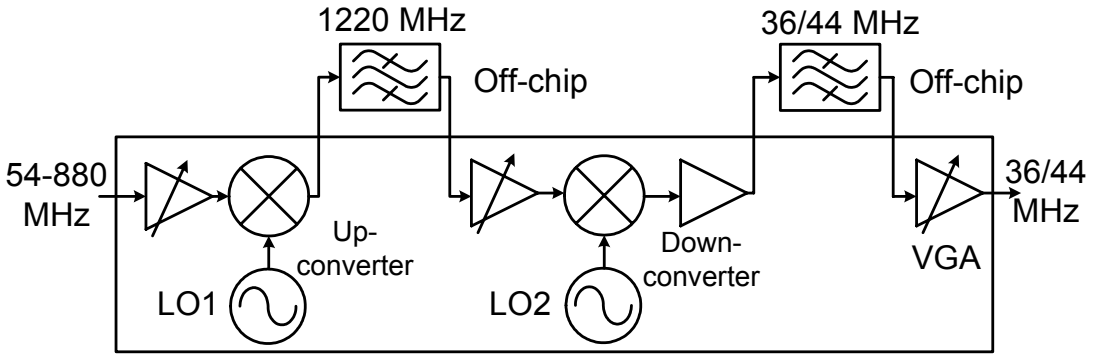

Fig. 2.2 Dual-conversion low-IF receiver for cable-TV tuners

2.2.4 Dual-Conversion Zero-IF Architecture

An alternative architecture well suited for integration of the entire transceiver is

the dual-conversion zero-IF architecture, which is shown in Fig. 2.3. In contrast to the direct-conversion zero-IF, the RF input signals are first converted to IF signals by LO1 frequency with single phase in the receiver. All the IF signals are then directly converted to zero-IF by second IQ LO2. The two-step frequency translation in the transmitter is realized in the opposite direction to the receiver chain. As in the case of direct-conversion, the adjacent channel rejection is accomplished by a baseband low-pass filter both for I and Q channels. This topology offers much flexibility in terms of the frequency planning of two LOs, with two steps convention available.

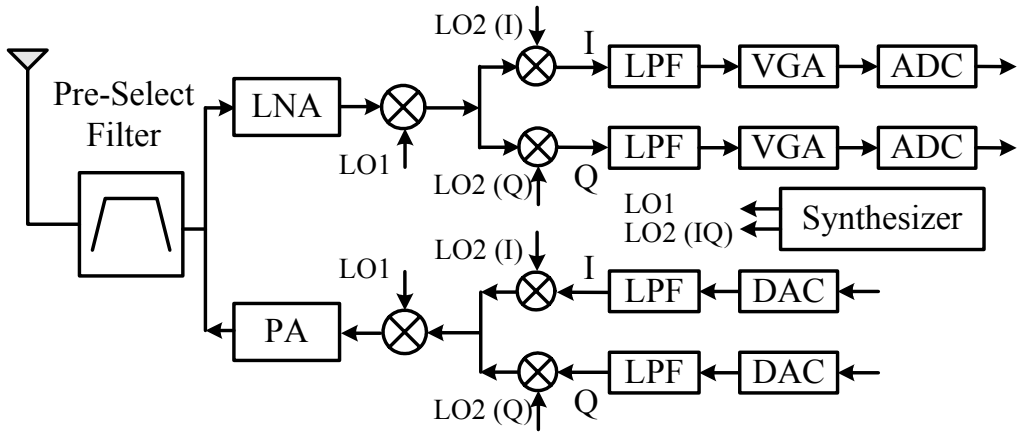

Fig. 2.3 Dual-conversion zero-IF transceiver architecture

In the first case, the first LO1 frequency could be fixed which translates all the input channels to a large bandwidth signal at IF. The channel selection is then realized with the tunable second IQ LO2 at lower frequency. This wideband IF scheme offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The foremost advantage is the fact that the channel tuning is performed using the second lower-frequency LO2. Consequently, the RF LO can be implemented by several techniques which allow the realization of low phase noise at output. In addition, since the tunable LO2 operates

at a lower frequency, the division ratio of the phase-locked loop in the frequency synthesizer is reduced, which not only implies a reduction in spurious tones generated by PLL but also results in better phase noise performance. However, this topology still faces the challenge of image rejection problem, which exists in the first setup conversion. Many techniques can be performed to deal with the image in narrowband systems, while the situation gets worse for wideband systems such as our 9-band UWB transceiver. The image signals occupy the same large bandwidth as input signals, and may fall into the design signal bands, which becomes really difficult to be attenuated. On the other hand, it is even hard to generate such wideband IQ LO2 at lower frequency.

In the second case, both the first LO1 and the second LO2 can be variable. Compared with the case of fixed LO1, the image bandwidth during first step conversion is reduced to trade off the requirement of both tunable LOs. That is also possible to generate both required tunable LO1 and LO2 from a single frequency synthesizer. As proposed in [9] for WLAN 11a system, the IQ LO2 is achieved with divided-by-4 from higher frequency LO1. This could be a suitable scheme for narrowband systems (e.g. WLAN 802.11a/b/g), but not for UWB systems because of both still wideband image and wideband IQ LOs problems there.

To deal with the image problem and avoid using wideband IQ LO signals for UWB systems, the third case LO scheme is proposed. The RF input channels are first down-converted to a fixed IF frequency band by first channel selection LO1. Instead of the tunable LO2 in the previous two cases, a fixed IQ LO2 is implemented with

the frequency equal to carrier frequency of the IF band. With this LO scheme, only one fixed frequency with IQ outputs is needed, which provides the advantage of guaranteed IQ phase accuracy. In addition, with careful frequency plan of LO1, the image bands can be pushed outside of the desired signal bands for easier filtering.

An additional advantage associated with the dual-conversion zero-IF architecture is that there are no local oscillators operating at the same frequency as the RF carriers. This not only eliminates the potential for the LO re-radiation problem that results in time-varying DC offsets, but also prevents the LO pulling. Although the second local oscillator is at the same frequency as the IF desired carrier in the dual-conversion zero-IF system, the offset which results at baseband from self-mixing is relatively constant and is easily cancelled. However, in the transmitter, since the 2nd-stage up-conversion mixer generates two sidebands, additional filtering following the mixer is needed to filter out the undesired sideband as well as some additional spurs.

Overall, the dual-conversion zero-IF transceiver architecture with fixed IQ LO2 scheme is the preferred choice for our 9-band UWB system. In the next section, the corresponding frequency planning and considerations are discussed.

2.3 Frequency Plan for 9-band MB-OFDM UWB Transceivers

2.3.1 General Considerations and Potential Solutions

As mentioned previously, a dual-conversion zero-IF architecture is adopted for our 9-band UWB transceiver to avoid a need for wideband and high-frequency IQ

LO signals, which would be required for the existing direct-conversion architecture. However, the image signals exist during the first-step conversion and need to be rejected. To achieve the require image rejection without sacrificing the power and complexity, carefully frequency planning has to be performed. On the one hand, the image bands should be located completely outside of the desired signal bands as well as further away from them allowing more image rejection by the RF filters. On the other hand, the required image rejection largely depends on the signal power presented in the image bands. As such, the designed image bands should avoid crossing with crowded frequency bands. In addition, the design complexity of the corresponding frequency synthesizer also needs to be taken into consideration.

Fig. 2.4 shows one of the possible frequency plans for the 9-band UWB system. The first four bands are down-converted to IF band at 2112 MHz by using lower-sideband oscillation LO1. In contrast to that, the highest five bands are translated to the same IF band as well, but with upper-sideband oscillation LO1. As shown in Fig. 2.4, the image bands are pushed to outside of the signal bands, and occupy two frequency bands from 0 to 1056 MHz and higher than 9504 MHz. Fig. 2.5 illustrates the block diagram of the frequency synthesizer for frequency plan 1. Nevertheless, this frequency plan introduces some critical challenges. Firstly, the band-pass filtering in front of the first-stage mixer is needed to reject the image signals at both sides of the signal bands. Whereas, it is more difficult to design a wideband LNA with band-pass characteristic to help the image rejection compared with low-pass. Thus, additional techniques have to be applied to achieve the required

image rejection. In addition, the GSM (900MHz) band is included in the low image band, which in fact raises the image rejection requirement of the system. Secondly, the two separated LO1 groups make the synthesizer's design challenging. A dual-wideband circuitry is necessary to drive the LO1 output signals. Consequently, the design complexity of the synthesizer is increased, which also results in the larger chip area and higher power consumption.

Fig. 2.6 and Fig. 2.7 present another possible frequency plan and its frequency synthesizer topology. However, because of the similar aforementioned reasons, this frequency plan faces too many challenges as well.

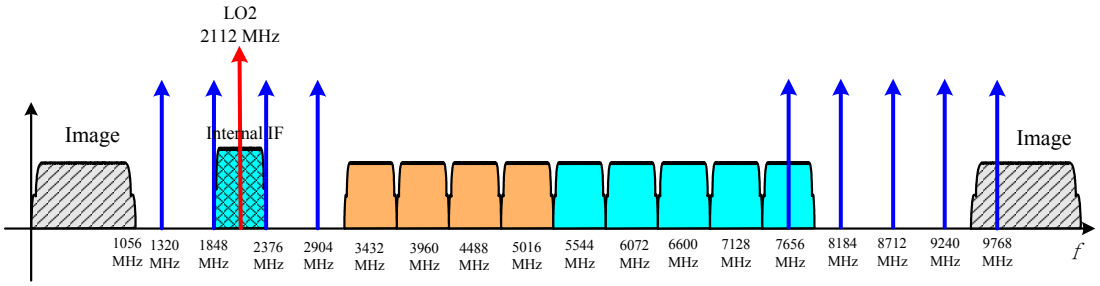

Fig. 2.4 Frequency plan 1 for 9-band UWB systems

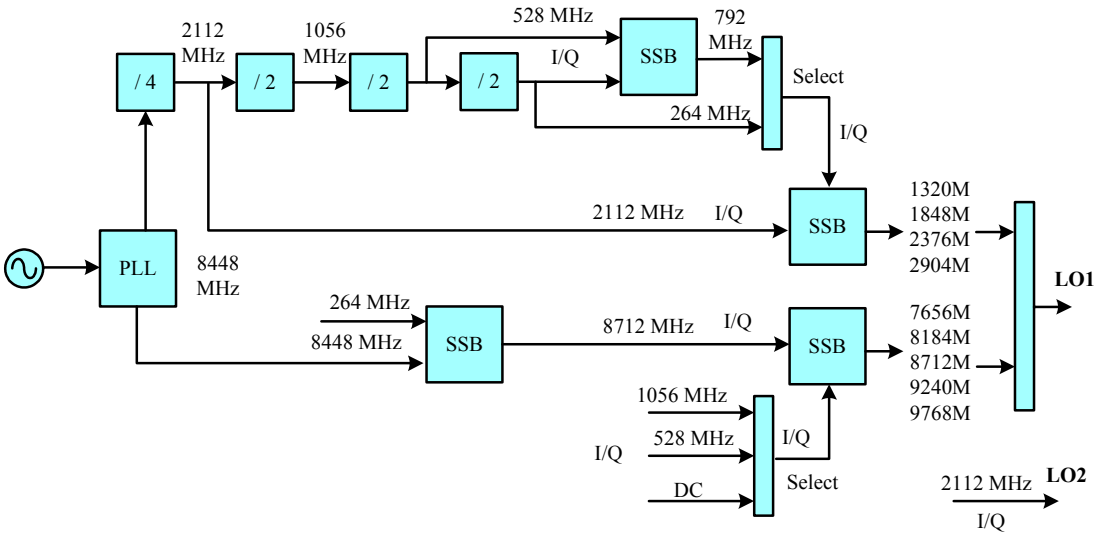

Fig. 2.5 Frequency synthesizer architecture for frequency plan 1

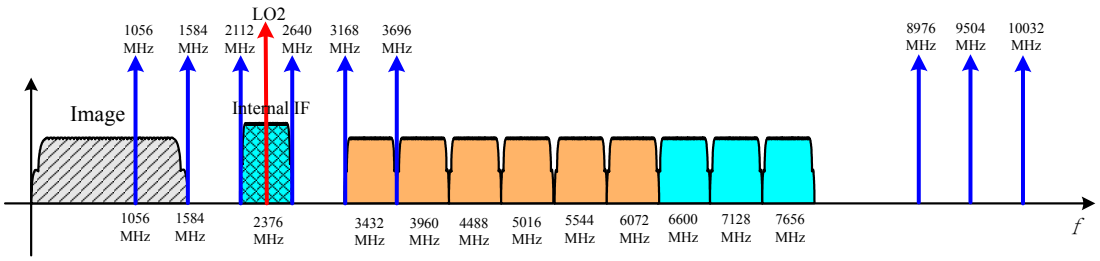

Fig. 2.6 Frequency plan 2 for 9-band UWB systems

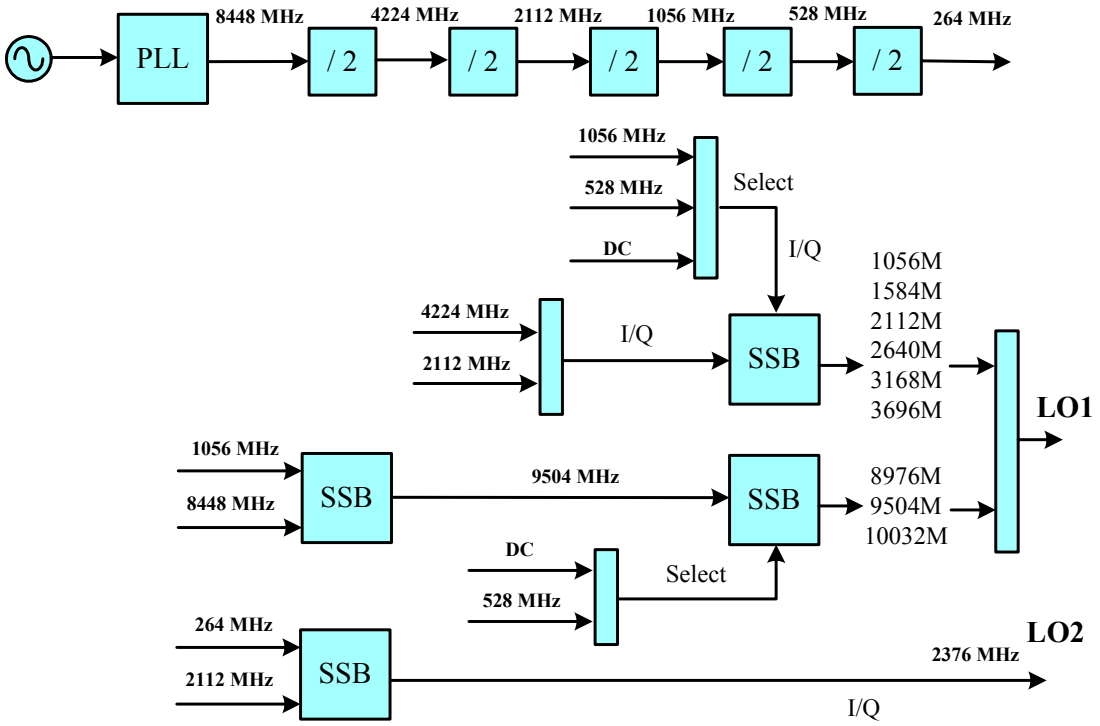

Fig. 2.7 Frequency synthesizer architecture for frequency plan 2

2.3.2 Proposed Dual-Conversion Zero-IF Frequency Plan

Instead of including both lower-sideband and upper-sideband LO1 for the first-step conversion in previous two possible frequency plans, the 9 bands can be down-converted with upper-sideband oscillation LO1 only. In reality, in our final proposed dual-conversion frequency scheme, upper-sideband oscillation with LO1 signals from 6.336 GHz to 10.56 GHz is proposed. A wideband circuitry is still needed to drive the wideband LO1, whereas it is more convenient to design a

continuous wideband circuitry than a dual-wideband one. In addition, with this proposed frequency scheme, the image frequency band is designed to be from 9 GHz to 13.7 GHz, which is completely outside of the desired signal band. Furthermore, some crowded frequency bands, such as GSM and ISM bands, are prevented lying in with the image band. With proper pre-filtering from the duplexer and the LNA, more than 30 dB image rejection can be easily achieved. As illustrated in Fig. 2.8, the first variable LO1 signal down-converts RF signals to a fixed IF1 frequency at 2.904 GHz, and the second fixed IQ LO2 signals further down-convert the IF1 signal to zero IF. As mentioned in the previous section, such a proposed scheme avoids a need for wideband and high-frequency IQ LO signals. Fig. 2.9 shows the block diagram of the proposed synthesizer associated with our proposed frequency scheme. All the required LO1 and IQ LO2 frequencies can be realized with single fully-integrated synthesizer.

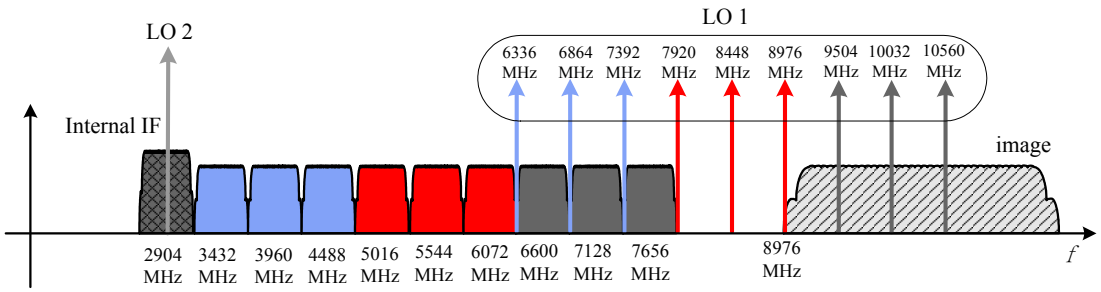

Fig. 2.8 Proposed dual-conversion frequency plan for 9-band UWB systems

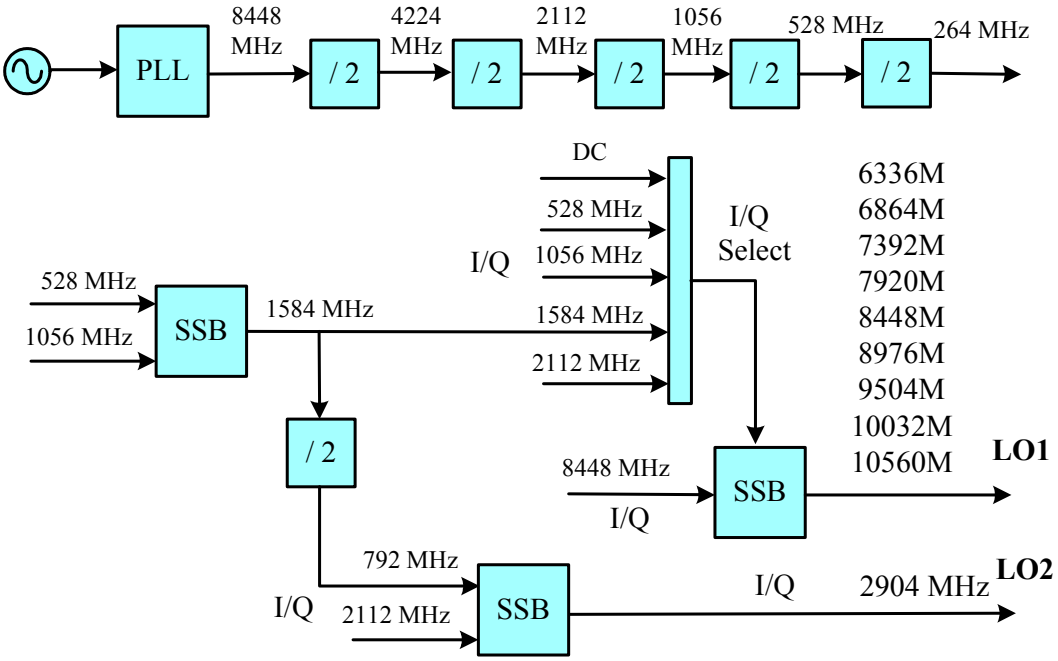

Fig. 2.9 Simplified synthesizer block diagram for the proposed frequency plan

2.4 Receiver and Transmitter Fundamentals

The function of a receiver is to successfully demodulate a desired signal in the presence of strong interferences and noises. In contrast, the purpose of a transmitter is to modulate the base-band data and then up-convert to a RF carrier frequency. In this section, some fundamental issues necessary to perform top level design and analysis of wireless receivers and transmitters are discussed, such as sensitivity, noise, non-linearity and EVM etc.

2.4.1 Basic Link Budget Analysis

- Channel Noise

For all communication systems, channel noise is intimately tied to bandwidth. All objects which have heat emit RF energy in the form of random (Gaussian) noise. The amount of noise can be calculated by:

$$N_{in}=10\log(KTB/1mW) \quad (2.1)$$

Where: N_{in} = Noise power (dBm)

K = Boltzman's constant (1.38×10^{-23} J/K)

T = System temperature, usually assumed to be 290K

B = Channel bandwidth (Hz)

This is the lowest possible noise level for a system with a given physical temperature.

- Range and Path loss

The received power is a function of the distance and the surrounding environment between the transmitter and the receiver. As radio waves propagate in free space, power falls off as the square of range. The path loss model in a free-space environment is given by:

$$P_L(f_g, d) = 20\log_{10}\left[\frac{4\pi f_g d}{c}\right] \quad (2.2)$$

Where f_g is defined as the geometric average of the lower and upper frequencies, d is the distance measured in meters, and c is the speed of the light.

$$f_g = \sqrt{f_{Lower} \cdot f_{Upper}} \quad (2.3)$$

- Signal-to-Noise Ratio (SNR)

For the purpose of link budget analysis, the most important aspect of a given modulation technique is the output Signal-to-Noise Ratio (SNR_{out}) necessary for a receiver to achieve a specified level of reliability in terms of bit error rate (BER) [10]. This is usually expressed as E_b/N_o, the energy in a single bit divided by the noise power in a single bit, which is independent of the system data rate. Top-level system

simulations can be performed to evaluate the minimum E_b/N_o in presence of channel losses. In order to convert from E_b/N_o to SNR_{out}, the data rate and system bandwidth must be taken into account as shown below:

$$SNR_{out} = 10\log[(E_b/N_o)\times(R/B)] \quad (2.4)$$

Where: E_b = Energy required per bit of information

N_o = Thermal noise in 1Hz of bandwidth

R = System data rate

B = Channel bandwidth

- Receiver Sensitivity

Receiver sensitivity is defined as the minimum signal threshold that can be detected in the presence of noises. It is computed by first estimating a required signal-to-noise ratio (SNR_{out}) for an acceptable system bit error rate (BER), as expressed by

$$Sens = N_{in} + NF + SNR_{out} \quad (2.5)$$

Where NF presents the input referred noise figure of the receiver

Based on the previous equations (2.1) and (2.4), equation (2.5) can be rewritten as

$$Sens = -174\ dBm/Hz + 10\log(B) + NF + E_b/N_o + R/B \quad (2.6)$$

2.4.2 Receiver Noise Analysis

RF circuits always suffer from noise problems including thermal noise, shot noise and flicker noise. All the noises introduced by each circuit in the receiver chain are accumulated at output, which significantly sacrifice the input sensitivity. In the receiver design, noise figure (NF) is commonly used to specify the noise

performance of the receiver system. The noise factor (F) is defined as the ratio of the input-SNR over the output-SNR of a system, as expressed by

$$F = SNR_{in} / SNR_{out} \tag{2.7}$$

The above equation in decibel becomes the noise figure

$$NF = 10\log(F) \tag{2.8}$$

Assume knowledge of the NF and gain of each block, the overall noise factor for a receiver with cascaded stages can be calculated by Frris equation expressed as follows

$$F_{tot} = F_1 + \frac{(F_2 - 1)}{A_{p1}} + \frac{(F_3 - 1)}{A_{p1}A_{p2}} + \cdots \tag{2.9}$$

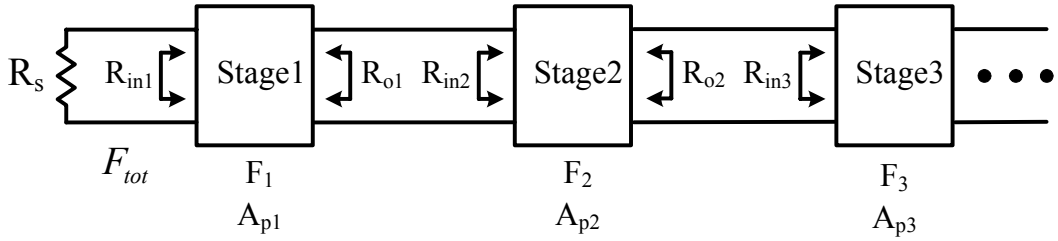

Fig. 2.10 Noise factor of cascaded stages

As illustrated in Fig. 2.10, F_i is the noise factor of the i^{th} stage and A_{pi} is the available power gain of the i^{th} stage. In a typical multi-component receiver, the input and output impedance of the RF blocks are matched to 50Ω. Consequently, the noise factor F_i is referred to a 50Ω impedance, and the power gain is then equal to the voltage gain. However, modern receivers are becoming increasingly more integrated, which allow unmatched impedance at the input and output of the receiver blocks. Therefore, some of the conventional definitions governing noise figure calculations can be confusing. In general, the 50Ω source impedance is assumed for the noise factor F_i in individual stage. However, the noise factor F_i in equation (2.9) should be

referred as the output impedance of the previous stage in an integrated receiver. This can be obtained from the equation shown below

$$NF_{(Ro,i-1)} = NF_{(50\Omega)} \times 50/R_{o,i-1} \tag{2.10}$$

In addition, the available power gain [11] is calculated by

$$A_{pi} = \left(\frac{R_{in,i}}{R_{o,i-1} + R_{in,i}} \right)^2 A_{vi}{}^2 \frac{R_{o,i-1}}{R_{o,i}} \tag{2.11}$$

where $R_{o,i-1}$ presents the output impedance of the previous stage, A_{vi} denotes un-loaded voltage gain of each stage. With information on the input and output impedances moving down the receiver chain, the receiver noise figure calculations and specifications are easily performed.

2.4.3 Receiver Linearity Analysis

Another key issue of the receiver design is its linearity. The receiver needs to satisfactorily extract the desired signal in the presence of strong adjacent channel and out-of-band interferers. If the receiver is inadequate in its frequency selection and linearity, it can degrade the desired signal by generating inter-modulation products. Generally, the level of this distortion determines the maximum power of an input signal that the receiver can process.

Third-order distortion is of particular importance in many of the receiver architectures, which is expressed in terms of third-order input intercept point IIP3. That defines the point where the extrapolated distortion products intercept with the fundamental tone in a two-tone test. Dependent on the location of the interferer tone, the IIP3 can be distinguished as in-band IIP3 and out-of-band IIP3. The IIP3 of the receiver can be found by:

$$\text{IIP3(dBV)} = P_{in} + (P_{out}\text{-}P_{IM3})/2 \tag{2.12}$$

where P_{in} and P_{out} are the input and output power level in dBV (dBV = dBm-13.01) respectively, and P_{IM3} is the power level of the undesired 3rd order inter-modulation product in dBV.

Another useful definition for compression or distortion is the 1-dB compression point, $P_{1\text{-dB}}$. The 1-dB compression point is defined as a point at which the voltage gain is down 1-dB from the ideal. It is approximated as follows:

$$P_{1-dB} \approx IIP3 - 10dB \tag{2.13}$$

Note that equation (2.13) is only true for In-band IIP3 without taking the filtering effect into account.

Given the information of IIP3 and voltage gain of each stage, the equivalent IIP3 of several cascaded stages can be found by

$$\frac{1}{(IIP3_{tot})^2} = \frac{1}{(IIP3_1)^2} + \frac{(A_{V1})^2}{(IIP3_2)^2} + \frac{(A_{V1}A_{V2})^2}{(IIP3_3)^2} + \cdots \tag{2.14}$$

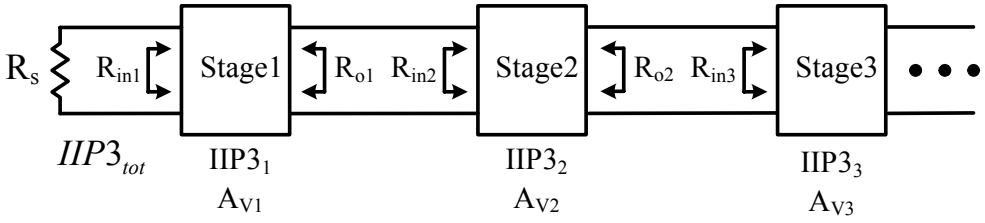

Fig. 2.11 Equivalent IIP3 of cascaded stages

As shown in Fig. 2.11, $IIP3_i$ and A_{Vi} present the input IIP3 and the loaded voltage gain of the i^{th} individual block respectively. In this approach, the assumption is that the distortion contribution from each of the blocks is uncorrelated.

2.4.4 Transmitter Constellation Diagram and EVM

Many modern transmitter systems widely use multi-carrier modulations like OFDM. One of the drawbacks is the large dynamic of the envelope of the modulated signal that makes it very sensitive to the distortions introduced by the nonlinearities of the transmitter path. The nonlinear effects are generally evaluated using parameters such as output 1-dB compression point ($OP_{1\text{-}dB}$) or Error Vector Magnitude (EVM). On the other hand, to aid in the visualizing of demodulated signals, constellation diagrams are often used to represent digital bits in terms of symbols. It is also a plot where each symbol is represented by a unique magnitude and phase. As shown in Figure 2.12, the error vector is the vector difference at a given time between the ideal symbol position and actual measured symbol position. The EVM is defined as the root-mean-square (RMS) of the error vector in a normalized constellation diagram [12].

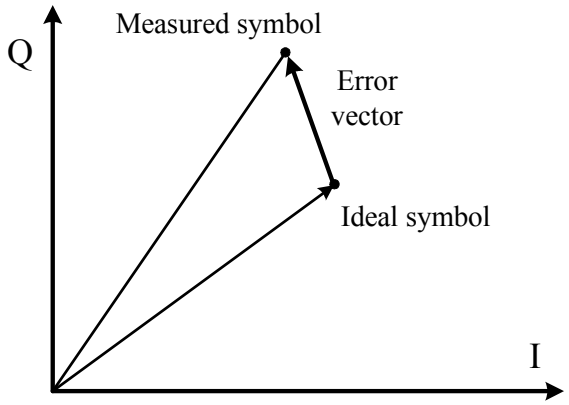

Fig. 2.12 Error vector magnitude

2.5 UWB Receiver Specifications

In order to launch a high-level design, it is necessary that all the system parameters are well studied and specified, in which the receiver NF, linearity and

voltage range requirements are especially critical for the receiver design.

2.5.1 UWB Receiver Link Budget

Table 2.1 shows the link budget for Mode 1 device (the first one groups with 3 bands), which is published in the MBOA proposal [13]. For a packet error rate (PER) of less than 8% with a PSDU of 1024 bytes, the minimum receiver sensitivity for a system operating at 110, 200, and 480 Mb/s is -80.5, -77.2, and -72.6 dBm, respectively. The column on the left is for the lowest data rate of 110 Mb/s and a range of 10 meters. That is the most challenging mode as the power received is extremely low due to the very significant path loss.

Table 2.1 Link Budget for first one groups (3 bands)

Parameter: Mode 1 DEV	**Value**	**Value**	**Value**
Information data rate (R_b)	110 Mb/s	200 Mb/s	480 Mb/s
Average Tx power (P_T)	–9.9 dBm	–9.9 dBm	–9.9dBm
Tx antenna gain (G_T)	0 dBi	0 dBi	0 dBi
$f_c^{'} = \sqrt{f_{\min} f_{\max}}$: geometric center frequency of waveform ($f_{\min}$ and $f_{\max}$ are the -10 dB edges of the waveform spectrum)	3882 MHz	3882 MHz	3882 MHz
Path loss at 1 meter ($L_1 = 20\log_{10}(4\pi f_c^{'} / c)$) $c = 3\times10^8$ m/s	44.2 dB	44.2 dB	44.2 dB
Path loss at d m ($L_2 = 20\log_{10}(d)$)	20 dB (d = 10 meters)	12 dB (d = 4 meters)	6 dB (d = 2 meters)
Rx antenna gain (G_R)	0 dBi	0 dBi	0 dBi
Rx power ($P_R = P_T + G_T + G_R - L_1 - L_2$ (dB))	–74.1 dBm	–66.1 dBm	–60.1 dBm
Average noise power per bit ($N = -174 + 10 * \log_{10}(R_b)$)	–93.6 dBm	–91.0 dBm	–87.2 dBm
Rx Noise Figure Referred to the Antenna Terminal (N_F)[1]	6.6 dB	6.6 dB	6.6 dB
Average noise power per bit ($P_N = N + N_F$)	–87.0 dBm	–84.4 dBm	–80.6 dBm
Required E_b/N_0 (S)	3.6 dB	4.3 dB	4.6 dB
Implementation Loss[2] (I)	2.9 dB	2.9 dB	3.4 dB
Link Margin ($M = P_R - P_N - S - I$)	6.4 dB	11.1 dB	12.5 dB
Proposed Min. Rx Sensitivity Level[3]	–80.5 dBm	–77.2 dBm	–72.6 dBm

[1] The primary sources for the noise figure are the LNA and mixer.

[2] Includes losses due to cyclic prefix overhead, front-end filtering, clipping at the DAC, ADC degradation, channel estimation, clock frequency mismatch, carrier offset recovery, carrier tracking, etc.

Here, we examine some of these critical parameters in the table to demonstrate how they were derived.

- TX Power

For OFDM implementations of UWB, the peak output is not constraining but the power density limits the output. The total transmitted power is the power density summed across the signal bandwidth. Recall that the FCC limits transmission to an EIRP of -41.25 dBm/MHz. In fixed frequency interleaving mode (FFI), the signal is transmitted on a single band. The total output power is then derived as

TX Power (Single Band) = -41.25 dBm/MHz + 10log(528MHz) = -14.1 dBm

In time-frequency interleaving mode (TFI), the signal hops among three bands multiple times during the measurement period within band groups. Consequently, the maximum TX power is calculated as

TX Power (Hopping) = -41.25 dBm/MHz + 10log(3×528MHz) = -9.3 dBm

- Path Loss

The path loss is a function of the frequency of the operation band as expressed by equations (2.2) and (2.3). For example, the total loss of the signal at 2m is calculated as P_L=50.2 dB.

- Receiver Sensitivity

For QPSK modulation and a BER of 1E-10, the required E_b/N_o is around 4.0 dB. From equation (2.6), the sensitivity at highest data rate is expressed by:

Sens = -174 dBm/Hz$+10\log(B)+10\log(R_{(480Mb/s)}/B)+NF+E_b/N_o$

where NF of 6.6 dB, and E_b/N_o of 4.6 are assumed, as a consequence

Sens = －174 dBm/Hz＋10log(480Mb/s)＋6.6＋4.6 = －76 dBm

By taking into account the implementation loss of 3.4 dB, the adjusted sensitivity is given by Sens = －72.6 dBm. The implementation loss includes losses due to cyclic prefix overhead, front-end filtering, clipping at the DAC, ADC degradation, channel estimation, clock frequency mismatch, carrier offset recovery, carrier tracking, etc.

- System Margin and Received Power

In the real application, we do not want to operate a receiver precisely at the limit of its sensitivity level. System margin is the additional received power over the minimum detectable power. Margin provides some headroom for design modifications and any tolerances that may exist in the transceiver system.

The received power is given by considering the transmit power, the gain of the transmitter and receiver antennas, and the path loss as given by

Rx_power = TX_power+Tx_Gain+Rx_Gain–Path_loss

For example, at the highest data rate of 480 Mb/s and the distance of 2 meters, the received power at the antenna is derived as:

Rx_power(2m, 480Mb/s) = – 9.9 – 50.2 = – 60.1 dBm

Consequently, the system margin is given by

System Margin = – 60.1 – (–72.6) = 12.5 dB

2.5.2 NF

As proposed by MBOA, a UWB receiver operated in only the first 3 bands (Mode 1 only) needs to have the noise figure of better than 6.6 dB, which is an

achievable value for low-cost CMOS process. Whereas, for the UWB device occupying the first 3 band groups with 9 bands, the required system NF (including external pre-selection filter) can be relaxed by 2 dB to 8.6 dB.

2.5.3 Selectivity and Linearity

The receiver linearity is set by the requirement that an in-band or out-of-band interferer does not cause a degradation of the signal-to-interference ratio (SIR). A minimum desired UWB signal is assumed to be 6 dB above the receiver sensitivity for an information data rate of 110 Mbps, which is –74.5 dBm. Based on the link budget table shown in Table 2.1, the average noise power per bit is -87 dBm. Since a margin of 6 dB is available, the sum of the interferer-and-noise power can be at most -81 dBm to maintain a PER<8% for a 1024 byte packet. Consequently, the maximum tolerable interferer power is around -82.3 dBm [13].

One of the largest out-of-band interferer powers at ISM band (IEEE 802.11b/g) could be up to –5.8 dBm at a minimum separation of 0.2m. Assuming the minimum attenuation provided by the front-end pre-select filter is 35 dB at 2.45 GHz, the interferer power at receiver LNA input is attenuated to –40.8 dBm. To meet the interferer power requirement (-82.3 dBm), extra 41.5 dB attenuation (@ 2.45 GHz) of the interference is needed in the receiver path. The aforementioned 802.11b/g interferer and the other out-of-band interference signals (such as PCS, GSM, etc.) mainly contribute to the P-1dB compression point required by the receiver. The effective P-1dB for these interferes is increased by the filtering in the RF and baseband receive chain. On the other hand, assuming a minimum communication

distance of 0.2m under fast frequency hopping mode, the maximum desired signal power received at input is -39.5 dBm. As a result, the preferred input P-1dB compression point of the receiver is around -23 dBm with enough margins [15].

In addition, the required in-band IIP3 of the receiver can be derived from equation (2.12), wherein two tones with maximum power of -39.5 dBm are assumed. It is calculated as IIP3 (dBm) = -39.5 dBm + (82.3-39.5)/2 dBm = -18.1 dBm. However, by considering the attenuation of the channel selection filters, the IIP3 requirement is relaxed.

2.5.4 Voltage Gain

The receiver chain is required to deliver a maximum voltage gain of 80 dB, such that peak of the UWB signal will reach the full-scale of the ADC input at the minimum sensitivity level. To cover the full dynamic range of input signals to the receiver, the gain must be variable over a 40dB range.

Table 2.2 summarizes the receiver specifications for the proposed UWB Transceiver

Table 2.2 Summary of the UWB receiver specifications

Data Rate	53.3Mb/s ~ 480 Mb/s	
Frequency Band	3168M~7920M (9 bands)	
Channel Bandwidth	528MHz	
Sensitivity	-80.8 dBm (53.3Mb/s)	-70.4 dBm (480Mb/s)
Receiver Gain	< 40 (Min gain) > 80 (Max gain)	
IIP3 (Out band)	> -13 dBm / -26 dBV (Min gain)	
IIP3 (In band)	> -19 dBm / -32 dBV (Min gain)	
IIP2 (In band)	> 20 dBm (Min gain)	
Input P-1dB	> -23 dBm (Min gain)	
Noise figure	< 8.6 dB (Max gain)	
Phase Noise of LO	-100dBc/Hz @ 1MHz	
Switching time	< 9ns	
Modulation	QPSK & DCM (>320Mb/s)	
PER	< 8%	
Supply Voltage	1.8 V	
Power consumption	200mA	
Process	TSMC 0.18-μm	

2.6 UWB Transmitter Specifications

On the transmitter side, the spectral mask and EVM both place restrictions on the linearity and spurs.

2.6.1 Output Spectrum

The transmitted spectral mask shall have the following break points: an emissions level of 0 dBr (dB relative to the maximum spectral density of the signal) from -260 MHz to 260 MHz around the center frequency, -12 dBr at 285 MHz

frequency offset, and -20 dBr at 330 MHz frequency offset and above. The transmitted spectral density of the transmitted signal shall fall within the spectral mask, as shown in Fig. 2.13 [13].

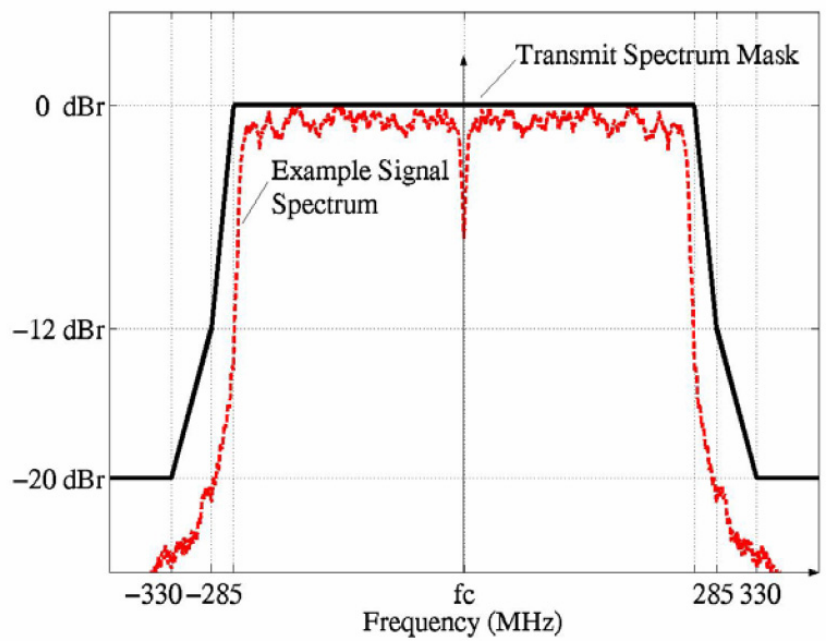

Fig. 2.13 Transmitter spectral mask

2.6.2 EVM

The relative constellation RMS error, averaged over all data and pilot sub-carriers of the OFDM symbols and over all of the frames, shall not exceed the values given in Table 2.3.

Table 2.3 Permissible relative constellation error

Data Rate (Mb/s)	Relative Constellation RMS Error (EVM)
53.3, 80, 106,7, 160, 200	-17.0 dB
320, 400, 480	-19.5 dB

The transmitter EVM is limited by thermal noise, DAC quantization noise, phase noise, IQ matching and linearity. ADS system simulation is first performed to define the linearity requirement of the transmitter with the following conditions:

Data rate: 480 Mb/s with Frequency Hopping.

Output power (dBm)	Input power (dBm)	Voltage Gain (dB)	OIP3 (dBm)	OP-1dB (dBm)	EVM (dB)
-9	-15	6	6	-4	-22.9

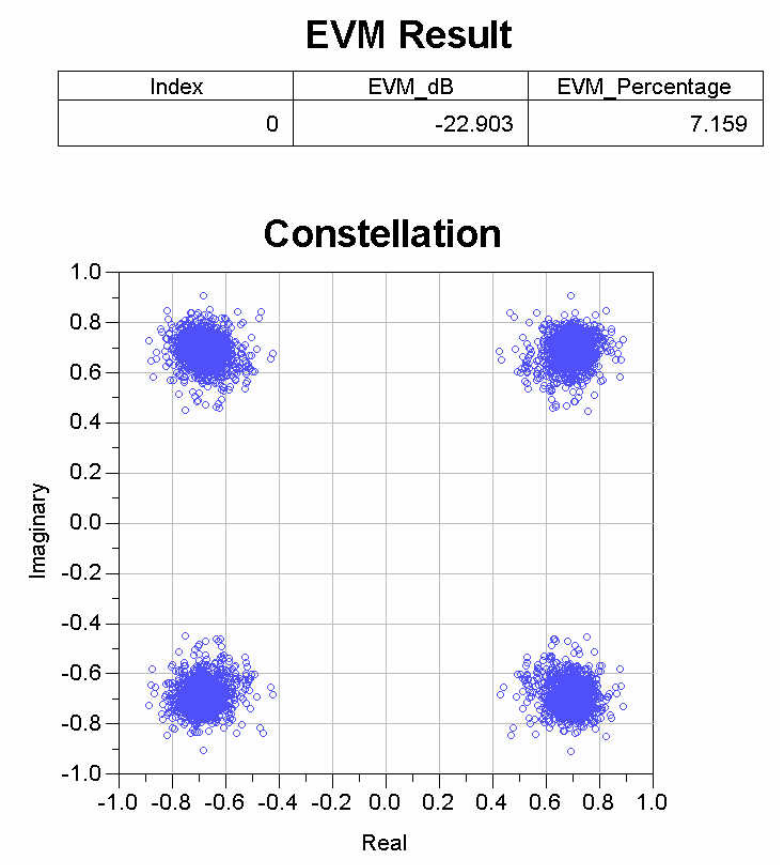

Fig. 2.14 Transmitter EVM from ADS Simulation

As illustrated in Fig. 2.14, an output 1dB compression point of -5 dB is required for the transmitter to meet the EVM requirement. Moreover, to make the IQ mismatch contribution to the overall EVM negligible, sideband rejection of better than -30 dB should be achieved [3].

2.7 Frequency Synthesizer Specifications

To sustain the proposed 9-band UWB transceiver with dual-conversion zero-IF

architecture, the frequency synthesizer needs to provide the first variable LO1 from 6.366 GHz to 10.56 GHz in steps of 528 MHz and the second LO2 at 2904 MHz with quadrature outputs. According to MBOA standard, the frequency synthesizer is imposed to have a fast band switching time of less than 9.5 ns for frequency hopping mode operation. To avoid conversion of strong out-of-band ISM band interferers (such as 802.11b/g and Bluetooth) into the wanted band, the spurious tones in the 5.35 GHz band should be below -45 dBc. For a similar reason, a better than -30 dBc sideband suppression is required to avoid conversion of unwanted band into the desired band. Finally, to ensure that the system SNR will not degrade by more than 0.1 dB due to inter-carrier modulation, the overall integrated phase noise should not exceed 3.5^{o} RMS [16]. Table 2.4 summarizes the specifications of the frequency synthesizer.

Table 2.4 Frequency synthesizer specifications

Synthesizer Parameters	Specification
LO1:	6336M, 6864M, 7392M, 7920M, 8448M, 8976M, 9504M, 10032M, 10560M
LO2:	2904M (I/Q)
Phase Noise	< -100 dBc @ 1M
Sideband Rejection	< -30 dBc
Output Power	400mVp-p single-end
Switching time	<9.5 ns
Supply Voltage	1.8 V
Power Consumption	<50mA
Process	TSMC 0.18-μm

2.8 Receiver Design Considerations and Building Blocks Specifications

The building blocks design in the receiver chain introduce many trade-offs in terms of total power consumption and overall performance. For instance, the overall receiver gain can be distributed over different stages. The larger gain at the first stage results in the relaxed NF requirement for the downstream stages while sacrificing the linearity. On the other hand, it depends on the spectral distribution of the unwanted neighbor signals and their signal level compared to the wanted signal. The more filtering is done in the early stages, the more relaxed linearity specifications become for the succeeding stages.

As a result, an RF band-pass band-selection filter from 3.1 GHz to 8 GHz should be employed in front of the LNA to perform preliminary filtering of the out-of-band interference. Further out-of-band filtering is accomplished not only by the LNA but also by a band-pass filter constructed by the LC-tank in the first-stage mixer. The channel-selection filtering is done by a low-pass filter before VGA. Recall that MBOA standard defines a total of 128 sub-carriers of 4.125 MHz each, wherein the 0th sub-carrier at DC is not used. Thereby, AC-coupling capacitors are connected at the output of the 2^{nd}-stage mixer and at the output of the channel-selection low-pass filter with overall corner frequency around 2 MHz to remove the dc offset.

2.8.1 LNA

Since the LNA sets the baseline NF of the receiver, NF of less than 5 dB (including the loss of the off-chip single-end-to-differential balun) is needed. In

addition, on the one hand, LNA is required to provide maximum gain of larger than 20 dB to suppress the NF contribution from later stages. On the other hand, to relax the linearity requirement of the coming building blocks, a LNA with reduced gain (12 dB) is preferred at maximum received power situation. The summary of the LNA specifications is shown in Table 2.5.

Table 2.5 Summary of LNA specifications

LNA parameters	Specification
Frequency Band	3168MHz~7920MHz
Voltage Gain	>20 dB (High Gain) <12 dB (low Gain)
Noise Figure (Max Gain)	< 5 dB
IIP3 (12 dB Gain, In band)	> -9 dBV
Supply Voltage	1.8 V
Power Consumption	< 20mA
Process	TSMC 0.18-μm

2.8.2 Down-Conversion Mixers

2 stage down-conversion mixers are needed to realize the proposed dual-conversion transceiver. In addition, to provide some out-of-band and adjacent channel rejection, a band-pass filter constructed by the LC-tank in the first-stage mixer should be implemented. The specifications of the two mixers are summarized in Table 2.6 and 2.7 respectively.

Table 2.6 First-stage mixer specifications

1st Mixer parameters	Specification
Input Frequency Band	3168 MHz~7920 MHz
Output frequency	2640MHz ~ 3168 MHz
Voltage Gain	2 dB
Noise Figure	< 17 dB
IIP3	> -2 dBV
Supply Voltage	1.8 V
Power Consumption	<6 mA
Process	TSMC 0.18-μm

Table 2.7 Second-stage mixer specifications

2nd Mixer parameters	Specification
Input Frequency Band	2640MHz ~ 3168 MHz
Output frequency	DC ~ 264 MHz
Voltage Gain	4 dB
Noise Figure	< 17 dB
IIP3	> -4 dBV
Supply Voltage	1.8 V
Power Consumption	< 6 mA
Process	TSMC 0.18-μm

2.8.3 RX-Filter

To further suppress the unwanted out-of-band interference and adjacent channel signal, around 3rd-order filtering at baseband is needed to achieve the adjacent-channel attenuation of better than -24 dBc, as specified in Table 2.8.

Table 2.8 RX-filter specifications

Rx-filter parameters	Specification
-3 dB Bandwidth	>260MHz
Low corner frequency	f<2 MHz
Attenuation	24 dB @ 528MHz
Order	~ 3rd order
Pass-band ripple	< 1 dB
Voltage Gain	5 dB
Noise Figure	< 18 dB
IIP3	> -4 dBV
Supply Voltage	1.8 V
Power Consumption	<25 mA
Process	TSMC 0.18-μm

2.8.4 VGA

In addition to the variable gain at the LNA stage, an AGC rang of 40 dB is implemented at analog baseband. Table 2.9 shows the specifications.

Table 2.9 VGA specifications

VGA parameters	Specification
-3 dB Bandwidth	> 260MHz
Low corner frequency	F < 2 MHz
Voltage Gain(Max)	50 dB
Voltage Gain(Min)	10 dB
Noise Figure	< 21 dB
Out P-1dB	> 6dBm (600mVp-p single end)
Supply Voltage	1.8 V
Power Consumption	< 20 mA
Process	TSMC 0.18-μm

2.8.5 ADC

According MBOA standard, the resolution of the A/D and D/A converters is lowered to around 5 bits.

Table 2.10 ADC specifications

A/D parameters	Specification
Resolution	6 bits
Sampling frequency	> 528M
SNR	> 30 dB
Supply Voltage	1.8 V
Power Consumption	< 50 mA
Process	TSMC 0.18-μm

2.9 Transmitter Design considerations and Building Blocks Specifications

There are significant differences between the design of receivers and transmitters. The input signal to the transmitter is a low frequency signal which contains only the information which has to be modulated. This signal is well known in shape, amplitude and power distribution. There are therefore not much trade-offs to be made during high-level design of the transmitter.

On the other hand, similar to the receiver chain, two-stage filtering is employed in transmitter part to remove the DAC alias and the unwanted spurs to fulfill the transmit mask requirement: a low-pass filter located at DAC output and an LC-tank filter at the output of the second-stage BB-IF1 up-conversion mixer. In addition, the RF band-selection filter at the output can also help to attenuate the unwanted

sideband introduced by IF1-RF conversation and the other out-of-band spurs as well. Thanks to the low transmit power requirement, a wideband PA can be eliminated. Instead, an output buffer stage is included to achieve both the desired power level and the required output matching.

2.9.1 DAC

To relax the attenuation requirement of transmitter filter, a sampling frequency up to 1.056 GHz is adopted, which is specified in Table 2.11.

Table 2.11 DAC specificationss

D/A parameters	Specification
Resolution	6 bits
Sampling frequency	528M ~ 1056M
SNR	>30 dB
Supply Voltage	1.8 V
Power Consumption	<20 mA
Process	TSMC 0.18-μm

2.9.2 TX-Filter

A transmitter analog filter is applied to remove the DAC alias. Table 3.12 presents the requirements.

Table 2.12 TX-filter specifications

TX-filter parameters	Specification
-3 dB Bandwidth	> 260MHz
Low corner frequency	f < 2 MHz
Attenuation	> 12 dB @ 1056MHz
Pass-band ripple	< 1 dB
Voltage Gain	0

2.9.3 Up-Conversion Mixers with Buffer

The overall specifications of the two stage up-mixers and buffer stage are summarized in Table 2.13.

Table 2.13 Up-mixer specifications

Up-Mixer parameters	Specification
RF Frequency	3168MHz~7920MHz
Voltage Gain	5 dB
Output P-1dB	-5 dBm
Supply Voltage	1.8 V
Power Consumption	<30 mA
Process	TSMC 0.18-μm

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Chapter 3 FREQUENCY SYNTHESIZER

3.1 Overview

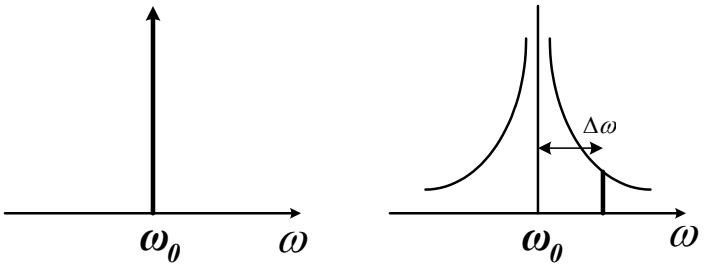
As discussed in Chapter 2, to implement the proposed dual-conversion zero-IF UWB transceiver covering the first 9 frequency bands from 3.1 to 8.0 GHz, a wideband synthesizer is required to generate the 1st LO1 signals from 6.336 GHz to 10.56 GHz in steps of 528 MHz and a fixed 2nd LO2 with IQ outputs at 2.904 GHz. In this chapter, the design and integration of the proposed fast-band-switching frequency synthesizer is presented. Each block in the synthesizer, including phase-locked loop, quadrature VCO, high-frequency multiplexer, and wideband single-sideband mixer are discussed in great detail. A proposed wideband inductive-network loading, a modified transformer-coupled quadrature VCO and long-metal-line loading-insensitive layout technique are analyzed as well. Finally, the measurement results of the proposed frequency synthesizer are shown.

3.2 Frequency Synthesizer Background

3.2.1 Definition of Phase Noise

Phase noise is characterized in the frequency domain. For an ideal oscillator operating at frequency ω_0, the output can be expressed as $V_{out}(t) = A \cdot \sin(\omega_0 t + \theta)$, where A is the amplitude and θ is an arbitrary phase reference. However, in a real oscillator the A ($A_{(t)}$) and θ ($\theta_{(t)}$) are functions of time [1]. Consequently, the output spectrum will have two sidebands close to the oscillation frequency, as illustrated in

Fig. 3.1.



(a) (b)

Fig. 3.1 Output spectrum of (a) an ideal oscillate, (b) a practical oscillator

The phase noise at an offset frequency Δω from carrier is defined as

$$L(\Delta\omega) = 10\log\left(\frac{p(\omega_0 + \Delta\omega)}{p(\omega_0)}\right) \tag{3.1}$$

where $p(\omega_0+\Delta\omega)$ presents the noise power in a 1-Hz bandwidth at frequency $\omega_0+\Delta\omega$, and $p(\omega_0)$ presents the carrier power. This is the single sided spectral noise density in units of decibel carrier per Hertz (dBc/Hz).

3.2.2 RMS Phase Error

In the time domain, the rising edges and falling edges of an oscillator output waveform do not always occur at exactly the time they should. As shown in Fig. 3.2, in contrast, they have a random phase error that can be either positive or negative. The standard deviation of this phase error is quantified as the RMS phase error, which is often referred as "phase jitter" as well.

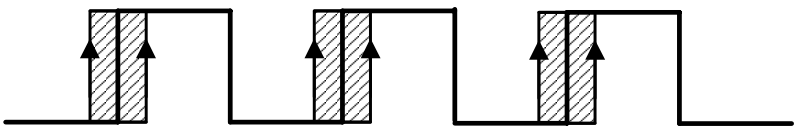


Fig. 3.2 RMS phase error in time domain

Recall that, in the frequency domain, phase noise is measured in dBc/Hz at a

specified frequency point, which hence can be treated as a phase noise density. To obtain the total phase error, the phase noise is integrated over the whole frequency spectrum. In addition, since the spectrum displays power vs. frequency, and not voltage vs. frequency, it is necessary to take the square root of the integrated product to obtain an RMS error. As a consequence, the RMS phase noise is calculated by converting from radians to degrees the square root of the integrated phase noise as illustrated by

$$RMSPhaseError = \frac{180}{\pi} \cdot \sqrt{2 \cdot \int_{a}^{b} L(f) \cdot df} \tag{3.2}$$

The limit, a, tends to be very close to the carrier, and the limit, b, tends to be much farther away, typically outside the loop bandwidth [2]. The factor of two is there to account for the phase noise on both sides of the carrier.

3.2.3 Synthesizer Architectures

One of the most commonly used frequency synthesizer architectures in RF transceiver applications is the indirect, phase-locked loop (PLL) based synthesizer. Fig. 3.3 shows the block diagram of the single-loop PLL based synthesizer, in which the voltage-control oscillator (VCO) output frequency is divided by a variable number N (or equivalent to N) in the variable divider. This divided frequency is then compared with the reference frequency in the phase and frequency detector (PFD), which gives an output signal equal to the phase difference between its two inputs. The signal is low-pass filtered by the loop filter, and is the control input to the VCO. Under locked condition, the two inputs of the PFD have a constant phase relationship. Therefore, the output frequency of the PLL is given by

$$f_{out} = N \times f_{ref} \tag{3.3}$$

where N denotes the equivalent division ratio of the variable divider.

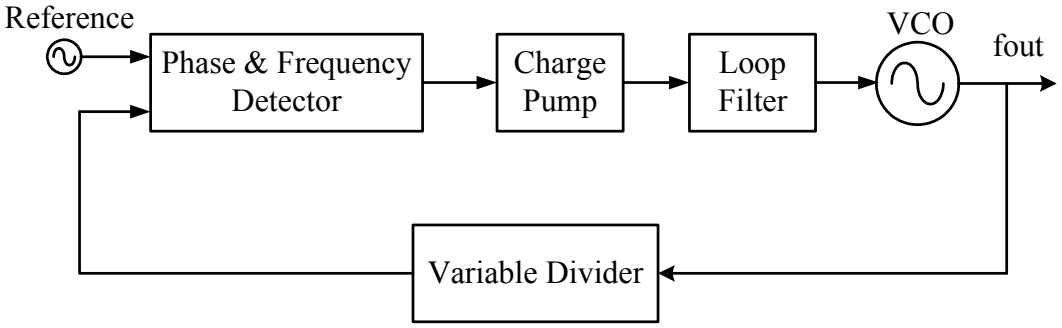


Fig. 3.3 Single-loop PLL frequency synthesizer

Moreover, depending on the equivalent division ratio of N, the PLL based synthesizer can be defined as integer-N synthesizers [3] and fractional-N synthesizers [4].

In the integer-N frequency synthesizer, the VCO frequency can only be at some integer multiple of the reference frequency. As a result, the reference frequency used in the synthesizer must be no higher than the desired channel spacing, or step size. This results in many problems for the system which has narrow channel spacing. Firstly, to assure a proper linear operation of the phase detector, the loop bandwidth must be limited to approximately one tenth of the value. The narrow loop bandwidth however will exhibit a slow transient response. Secondly, lower reference frequency implies a larger division ratio of N, which results in a worse phase noise.

In contrast, the fractional-N frequency synthesizer allows the loop to lock the VCO to a frequency that is a fractional multiple of the reference frequency, which is realized by switching very fast between two divider moduli X and X+1. This, in turn, allows the use of a comparison frequency larger than the step size. Thus, the division

ratio can be small, and the system phase noise can be improved as well. Nevertheless, the technique also has its disadvantages. The most critical one is the generation of fractional spurs in the output spectrum, because the division ratio is toggled between X and X+1 continuously. Of course, that can be improved by many techniques. For example, ΣΔ modulator can be applied to randomize the divider moduli selection [5].

In contrast to the single-loop PLL synthesizer, the dual-loop synthesizer [6] adds a low variable frequency from a low-frequency PLL to a high fixed offset frequency generated from a second high-frequency PLL, which is illustrated in Fig. 3.4. The frequency change of the synthesizer therefore only requires the change of a small division ratio in the low-frequency PLL. The resulting output frequency is expressed by

$$f_{out} = M \times f_{ref1} \pm \frac{N \times f_{ref2}}{X} \tag{3.4}$$

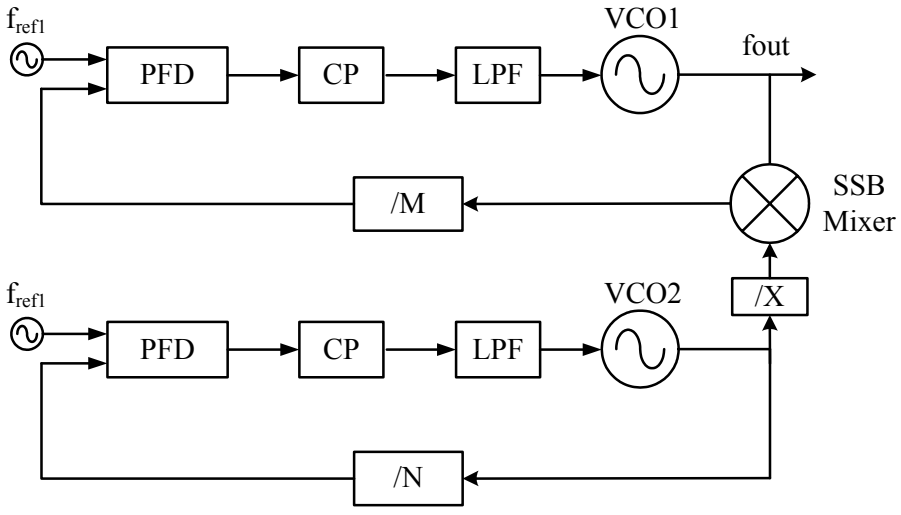


Fig. 3.4 Block diagram of the dual-loop synthesizer

This dual-loop architecture can improve the tradeoff among phase noise, channel spacing, reference frequency, and locking speed of the synthesizer, which exist in the

single-loop synthesizer. In addition, by placing the SSB mixer inside the feedback loop, the unwanted sidebands at the mixer output resulting from mismatches and nonlinearities of the SSB mixing are significantly suppressed by the divider and the low-pass filter of the high-frequency loop.

The aforementioned indirect, phase-locked synthesizers, however, are inherently slow to settle down. Changing the frequency is accomplished by changing the division ratio, which results in a slow change of the VCO control voltage as the loop acquires its steady-state operation. Therefore, in the order of micro second (us) setting time is typically needed for these indirect synthesizers. As such, the indirect architecture is incapable of providing a fast-switching time of less than 9.5ns which is required for UWB systems. To achieve the desired fast frequency switching, the direct synthesizer architecture can be applied, where a SSB mixer is applied at outside of the loop for direct frequency mixing. The fixed frequency generated from a high frequency-PLL is synthesized with other switch-able low frequencies by SSB mixing. Thanks to the open loop synthesis of the output frequency, fast switching time of nanosecond is expected.

3.3 Proposed Frequency Synthesizer for 9-band UWB Transceivers

One of the stringent requirements in the MB-OFDM UWB specification is that the channel switching time should be less than 9.5 ns. As mentioned in previous sections, it is impossible for the conventional phase-locked-loop-based synthesizer to achieve. On the other hand, a SSB-mixer-based frequency synthesizer is a suitable

choice. The proposed UWB synthesizer employs a high-frequency PLL with a fixed output frequency and wideband SSB mixers (WB-SSB) employing a proposed wideband inductor network, as shown in Fig. 3.5. An on-chip PLL with quadrature VCO and an external reference of 66 MHz is implemented to generate 8.448-GHz IQ outputs as the fundamental frequency for the synthesizer. In order to achieve the 6.336 GHz to 10.56 GHz LO1, the 8.448-GHz IQ signals are applied to the WB-SSB mixer to mix with another input whose frequency is switch-able. The synthesizer's output frequencies are given as

$$f_{LO1} = 8.448G \pm (0,528M,1.056G,1.584G,2.112G) \tag{3.5}$$

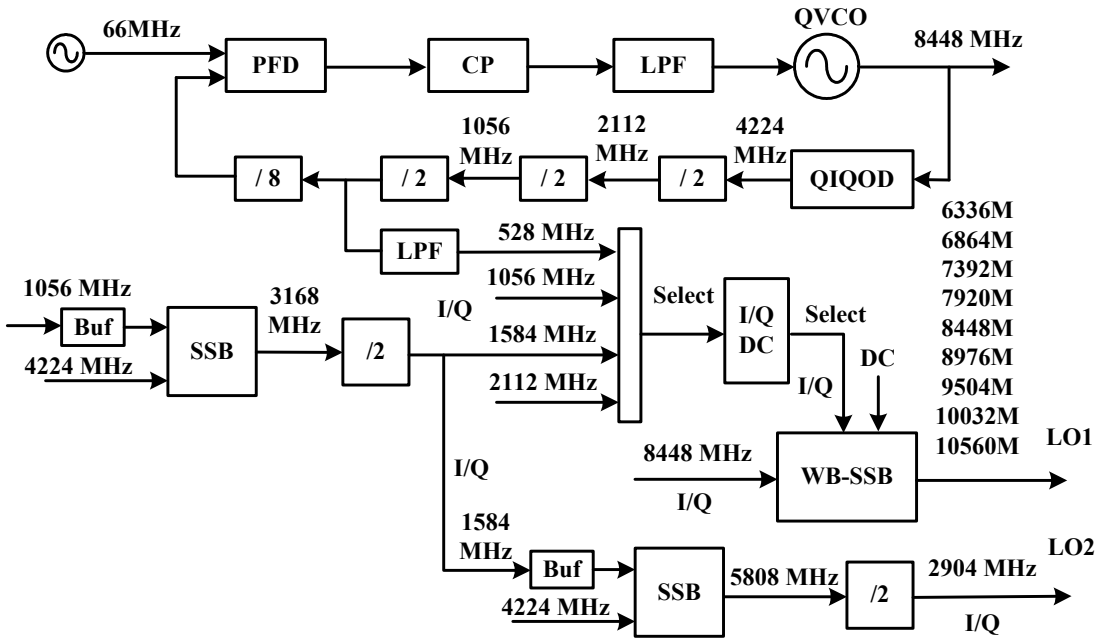


Fig. 3.5 Block diagram of the proposed frequency synthesizer

As illustrated in Fig. 3.5, all the switched input frequencies for WB-SSB Mixer can be derived from the fundamental frequency of the quadrature VCO outputs, and divide-by-2 dividers are used to produce IQ signals for all synthesized frequencies for high phase accuracy. The required 2.904-GHz IQ LO2 signals are also obtained

from a combination of single-sideband mixers and divide-by-2 dividers.

A 3-stage fast band-switching scheme is proposed. A frequency multiplexer (MUX) and an IQ phase MUX are implemented sequentially, followed by a DC mixing selection at the WB-SSB mixer stage. The band selection is accomplished by switching the wideband inductive-network to the desired band and simultaneously switching the WB-SSB input to the desired frequency and phase. Fast switching can be achieved since they can operate simultaneously. A simple 3-stage RC low pass filter is added to attenuate the third harmonic of the 528 MHz signals at 1584 MHz, which is one of the in-band mixed frequencies.

3.4 Phase-Locked Loop Design

As mentioned previously, an on-chip PLL with quadrature VCO is needed to deliver a fundamental frequency at 8.448 GHz. The designed PLL is expected to achieve an integrated phase noise of 3.5 degree RMS. This session presents the detailed analysis and design of the phase-locked loop, from system to circuit level.

3.4.1 System Design and Calculation

To eliminate the steady-state phase error, as well as to achieve enough spur suppression, a type II charge pump based PLL with 4^{th}-order is adopted for this application, which is shown in Fig. 3.6. Wherein, a series resistor R3 and a shunt capacitor C3 prior to the VCO are added to provide a low-pass pole for additional attenuation of unwanted spurs. In addition, a dual-path active loop filter [6] is used to minimize the total capacitance, so as to minimize the chip area.

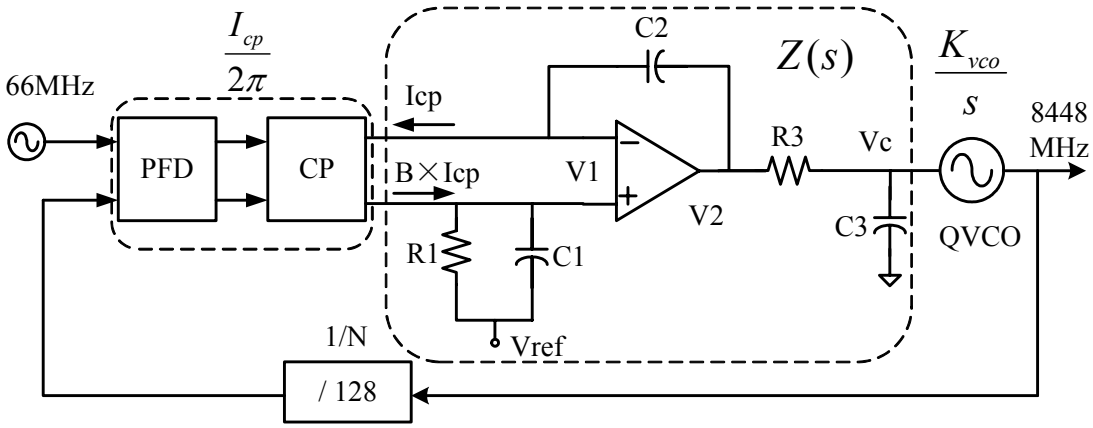


Fig. 3.6 Block diagram of the PLL in the proposed synthesizer

In a closed-loop system, the loop stability is one of most important items that we need to study in great detail. Open loop analysis is used to analyze the performance of the PLL. Consequently, the parameters of the loop filter can be derived.

As shown in Fig. 3.6, the loop filter is driven by two charge pump output currents with different current levels of $-I_{cp}$ and $B\times I_{cp}$. With some simple calculations, the transfer function of the 3rd-order loop filter is expressed by

$$\frac{V_c}{I_{cp}} = \frac{1}{sC_2}\cdot\frac{1+sR_1(C_1+B\cdot C_2)}{1+sR_1C_1}\cdot\frac{1}{1+sR_3C_3} \tag{3.6}$$

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$\tau_Z = R_1(C_1+B\cdot C_2);\ \ \tau_{p1} = R_1C_1;\ \ \tau_{p3} = R_3C_3 \tag{3.7}$$

By substituting (3.7) into (3.6), we have

$$Z(s) = \frac{V_c}{I_{cp}} = \frac{1}{sC_2}\cdot\frac{1+s\tau_Z}{1+s\tau_{p1}}\cdot\frac{1}{1+s\tau_{p3}} \tag{3.8}$$

Thus, the open loop gain of the PLL can be calculated as

$$G_o(s) = \frac{I_{cp}K_{VCO}}{2\pi \cdot NC_2} \cdot \frac{1+s\tau_Z}{s^2\left(1+s\tau_{p1}\right)} \cdot \frac{1}{1+s\tau_{p3}} \tag{3.9}$$

$$G_o(j\omega) = \frac{I_{cp}K_{VCO}}{2\pi \cdot NC_2} \cdot \frac{1+j\omega\tau_Z}{-\omega^2\left(1+j\omega\tau_{p1}\right)} \cdot \frac{1}{1+j\omega\tau_{p3}} \tag{3.10}$$

where K_{VCO} presents the VCO gain constant in unit of rad/V and I_{cp} presents the charge pump current. Consequently, the phase and the phase margin of the loop are calculated in (3.11) and (3.12) respectively

$$Phase = \phi(\omega) = -180^0 + \tan^{-1}\left(\omega\tau_Z\right) - \tan^{-1}\left(\omega\tau_{p1}\right) - \tan^{-1}\left(\omega\tau_{p3}\right) \tag{3.11}$$

$$PM = \tan^{-1}\left(\omega\tau_Z\right) - \tan^{-1}\left(\omega\tau_{p1}\right) - \tan^{-1}\left(\omega\tau_{p1}\right) \tag{3.12}$$

By setting the differentiation of the phase equal to zero, Equation (3.11) is rewritten as

$$\frac{d\phi(\omega)}{d\omega} = \frac{\tau_Z}{1+\left(\omega\tau_Z\right)^2} - \frac{\tau_{p1}}{1+\left(\omega\tau_{p1}\right)^2} - \frac{\tau_{p3}}{1+\left(\omega\tau_{p3}\right)^2} = 0 \tag{3.13}$$

It is well known that the corresponding frequency point expressed by Equation (3.13) implies a peak value of the phase. On the other hand, the two poles, p_1 and p_3, are usually designed at the same location. That means

$$\tau_{p1} = \tau_{p3} \tag{3.14}$$

Thus, Equation (3.12) can be rearranged as

$$\left[1-\left(\omega\tau_p\right)^2\right]\left[\omega\tau_Z - \tan(PM)\right] - 2\omega\tau_p\left[1+\omega\tau_Z\tan(PM)\right] = 0 \tag{3.15}$$

To ensure good loop stability, the phase margin should be maximized when the magnitude of the open loop gain equals to 1, as illustrated in Fig. 3.7.

Therefore, as long as the phase margin PM and loop bandwidth $\omega = \omega_c$ are specified, Equations (3.13) to (3.15) allow us to calculate the two constants, τ_Z and $\tau_p = \tau_{p1} = \tau_{p3}$. Moreover, at loop bandwidth point we have

$$\left|G_o(j\omega)\right|_{\omega=\omega_C} = \left|\frac{I_{cp}K_{VCO}}{2\pi \cdot NC_2} \cdot \frac{1+j\omega\tau_Z}{-\omega^2\left(1+j\omega\tau_{p1}\right)} \cdot \frac{1}{1+j\omega\tau_{p3}}\right| = 1 \tag{3.16}$$

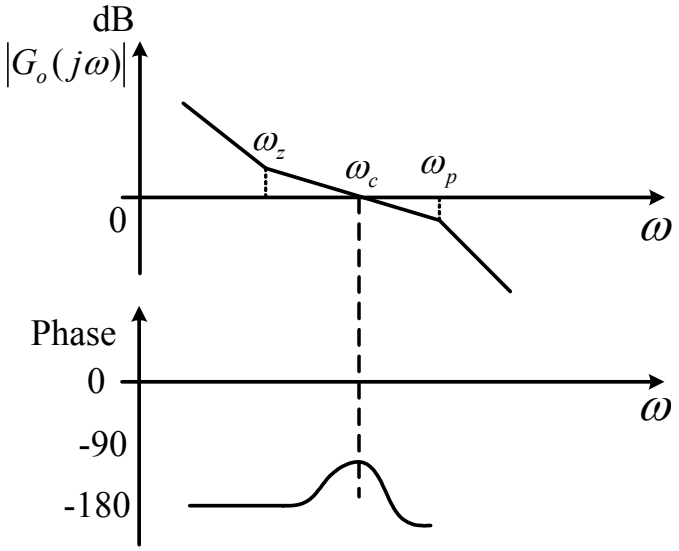


Fig. 3.7 Open loop response Bode plot

As a result, the parameters of the loop filter can be derived as

$$C_2 = \frac{I_{cp}K_{VCO}}{2\pi \cdot N\omega_c^{\,2}} \cdot \frac{\sqrt{1+\left(\omega_c\tau_Z\right)^2}}{1+\left(\omega_c\tau_p\right)^2} \equiv K_1 \cdot I_{cp} \tag{3.17}$$

$$R_1 = \frac{\tau_Z - \tau_p}{B \cdot C_2} = \frac{\tau_Z - \tau_p}{B \cdot K_1 \cdot I_{CP}} \tag{3.18}$$

$$C_1 = \frac{\tau_p}{R_1} = \frac{B \cdot C_2 \cdot \tau_p}{\tau_Z - \tau_p} = \frac{B \cdot K_1 \cdot I_{CP} \cdot \tau_p}{\tau_Z - \tau_p} \tag{3.19}$$

$$R_3 = \frac{R_1}{K_{c13}} = \frac{\tau_Z - \tau_p}{K_{c13} \cdot B \cdot K_1 \cdot I_{CP}} \tag{3.20}$$

$$C_3 = K_{c13} \cdot C_1 = \frac{K_{c13} \cdot B \cdot K_1 \cdot I_{CP} \cdot \tau_p}{\tau_Z - \tau_p} \tag{3.21}$$

where $$K_1 \equiv \frac{K_{VCO}}{2\pi \cdot N\omega_c^{\,2}} \cdot \frac{\sqrt{1+\left(\omega_c\tau_Z\right)^2}}{1+\left(\omega_c\tau_p\right)^2} \tag{3.22}$$

And K_{c13} is the capacitor ratio of C_3 to C_1.

Moreover, from the above equations, it can be seen that factor B helps to reduce the value of C_2 for a given value of R_1. As such, the chip area of the loop filter can be

decreased with the expense of the filter complexity.

3.4.2 Phase Noise Contribution Analysis

In general, all the loop elements in the PLL, including the charge pump, the LPF and the VCO generate noises which contribute to the overall phase noise of the PLL. However, different components in the loop show various kinds of spectrums exhibiting low-pass, band-pass or high-pass characteristics as they are propagated to the output. Fully understanding of the noise contribution from each part of the PLL becomes critical in the design. The main noise distributions of the loop are illustrated in Fig. 3.8.

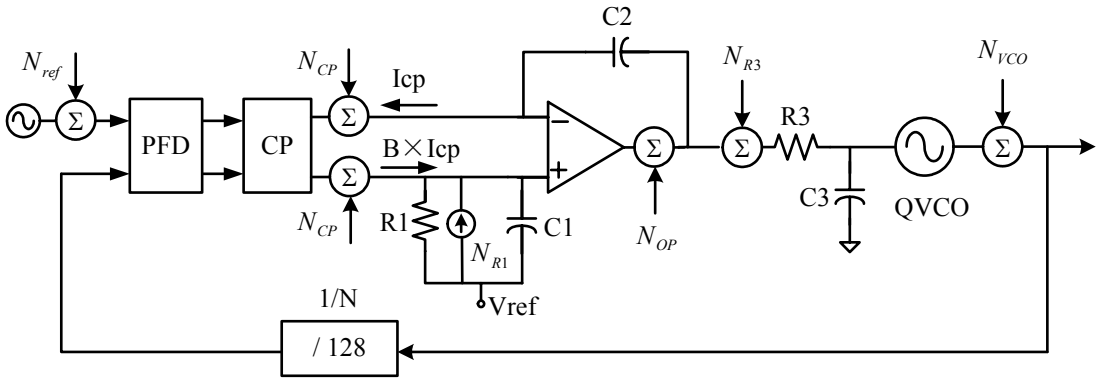


Fig. 3.8 Block diagram of the noise distribution in the PLL

To simplify the following analysis, two transfer functions are first denoted as

$$H_1(s) = \frac{R_1}{1 + s\tau_{p1}} = \frac{R_1}{1 + sR_1C_1} \tag{3.23}$$

$$H_3(s) = \frac{1}{1 + s\tau_{p3}} = \frac{1}{1 + sR_3C_3} \tag{3.24}$$

By substituting (3.17) into (3.9), the open loop transfer function is rearranged as

$$G_o(s) = K_0 \cdot \frac{1 + s\tau_Z}{s^2\left(1 + s\tau_{p1}\right)} \cdot \frac{1}{1 + s\tau_{p3}} \tag{3.25}$$

where $$K_0 \equiv \frac{I_{cp} K_{VCO}}{2\pi \cdot NC_2} = \frac{\omega_c{}^2 \cdot \left(1+(\omega_c \tau_p)^2\right)}{\sqrt{1+(\omega_c \tau_Z)^2}} \tag{3.26}$$

- VCO noise contribution

The composite noise contribution from the VCO to the PLL output is computed as

$$L_{VCO} = N_{VCO}(s)\left(\frac{1}{1+G_0(s)}\right)^2 \tag{3.27}$$

where $N_{VCO}(s)$ denotes the single-sideband (SSB) noise of the VCO.

As can be seen from Equations (3.25) and (3.27), the noise of the VCO is effectively high-pass filtered by the PLL loop, which mainly contributes to the out-of-band noise. It implies that the loop bandwidth should be sufficiently wide to eliminate the VCO noise contribution.

- Input reference noise contribution

In contrast to the VCO, the input reference noise contribution shows a low-pass characteristic, as expressed by

$$L_{ref} = \frac{1}{2} N_{ref}(s)\left(\frac{N \cdot G_0(s)}{1+G_0(s)}\right)^2 \tag{3.28}$$

The reference noise is amplified by the loop division ratio of N within the bandwidth of the PLL, but attenuated above this frequency. In order to minimize this noise, the loop bandwidth must be as small as possible, a requirement in conflict with that of the case from the VCO.

- Loop opamp noise contribution

The single-sided phase noise transfer function contributed by the loop opamp is

$$L_{op} = \frac{1}{2} N_{op}(s) \left(\frac{\frac{K_{VCO}}{s} \cdot H_3(s)}{1 + G_0(s)} \right)^2 \tag{3.29}$$

where $N_{op}(s)$ is the input referred voltage noise of the opamp in unit of V^2/Hz.

- Loop filter resistor R3 noise contribution

The resistor R3 in the loop filter also generates white noise $N_{R3}=4kT \cdot R_3$ that will have a contribution on the output phase noise as well. The single-sided phase noise transfer function is expressed by

$$L_{R3} = \frac{1}{2} \cdot 4KTR_3 \left(\frac{\frac{K_{VCO}}{s} \cdot H_3(s)}{1 + G_0(s)} \right)^2 = \frac{1}{2} \cdot 4KT \cdot \frac{(\tau_Z - \tau_p) \cdot K_{VCO}}{K_{c13} \cdot B \cdot K_2 \cdot I_{CP}} \left(\frac{H_3(s)}{s(1 + G_0(s))} \right)^2 \tag{3.30}$$

where

$$K_2 \equiv \frac{1}{2\pi \cdot N\omega_c^{\,2}} \cdot \frac{\sqrt{1 + (\omega_c \tau_Z)^2}}{1 + (\omega_c \tau_p)^2} \tag{3.31}$$

- Loop filter resistor R1 noise contribution

In contrast to R3, the white noise from resistor R1 can be modeled as current noise. Therefore, the single-sided phase noise transfer function contributed by the loop resistor R1 is given by

$$\begin{aligned} L_{R1} &= \frac{1}{2} \cdot \frac{4KT}{R_1} \left(\frac{\frac{K_{VCO}}{s} \cdot H_1(s) \cdot H_3(s)}{1 + G_0(s)} \right)^2 \\ &= \frac{1}{2} \cdot 4KT \cdot \frac{(\tau_Z - \tau_p) \cdot K_{VCO}}{B \cdot K_2 \cdot I_{CP}} \cdot \left(\frac{H_3(s)}{s \cdot (1 + s\tau_{p1}) \cdot (1 + G_0(s))} \right)^2 \end{aligned} \tag{3.32}$$

- Charge Pump noise contribution

As shown in Fig. 3.8, two charge pumps are needed in the dual-loop filter. Thereby,

the charge pump noise transfer function consists of two parts, as expressed in Equation (3.33).

$$\begin{aligned} L_{CP} &= \frac{1}{2}\cdot N_{CP}(s)\left[B\cdot\left(H_1(s)\right)^2+\left(\frac{1}{sC_2}\right)^2\right]\left(\frac{\frac{K_{VCO}}{s}\cdot H_3(s)}{1+G_0(s)}\right)^2 \\ &= \frac{1}{2}\cdot 4KT\cdot\frac{2}{3}\cdot\frac{2\cdot I_{CP}}{\left(V_{gs}-V_{th}\right)}\cdot\lambda_{on}\cdot\left[B\cdot\left(H_1(s)\right)^2+\left(\frac{1}{sC_2}\right)^2\right]\left(\frac{\frac{K_{VCO}}{s}\cdot H_3(s)}{1+G_0(s)}\right)^2 \end{aligned} \tag{3.33}$$

By substituting (3.17) into (3.33), we have

$$L_{CP} = \frac{1}{2}\cdot 4KT\cdot\frac{2}{3}\cdot\frac{2}{\left(V_{gs}-V_{th}\right)\cdot {K_2}^2\cdot I_{CP}}\cdot\lambda_{on}\cdot\left[\frac{\left(\tau_Z-\tau_p\right)^2}{\left(1+s\tau_{p1}\right)^2}\cdot\frac{1}{B}+\left(\frac{1}{s}\right)^2\right]\left(\frac{H_3(s)}{s\left(1+G_0(s)\right)}\right)^2 \tag{3.34}$$

where λ_{on} is the switch-on duty cycle of the charge pumps. In the locked scenario, the noise contribution is reduced by this λ_{on} factor because the noise sources are active only for a small duration over a reference period.

The above analysis shows that the phase noise contributions from loop resistors R1, R3 and charge pump can be reduced by increasing the charge pump current. Nevertheless, the capacitance and chip area of the loop filter increases proportionally with the increase of charge pump current. On the other hand, it can be found that the in-band phase noise is dominated by the external reference, the charge pump, and the loop filter, while the out-band phase noise is limited by the free-running phase noise of the VCO. In addition, it is noted that the close-in phase noise contribution of each noise source is enlarged by the division ration N or N^2. The noise power is also amplified by a factor of K_{VCO} or K_{VCO}^2. To reduce the division ratio N, an achievable external reference of 66 MHz is selected, which results in a division ratio of 128 in

our proposed PLL.

Recall that the PLL is expected to achieve a RMS noise of 3.5 degree. Fig. 3.9 shows a typical phase noise output spectrum of a PLL, in which the phase noise reduction of 20 dB/decade starting from the loop band width is assumed.

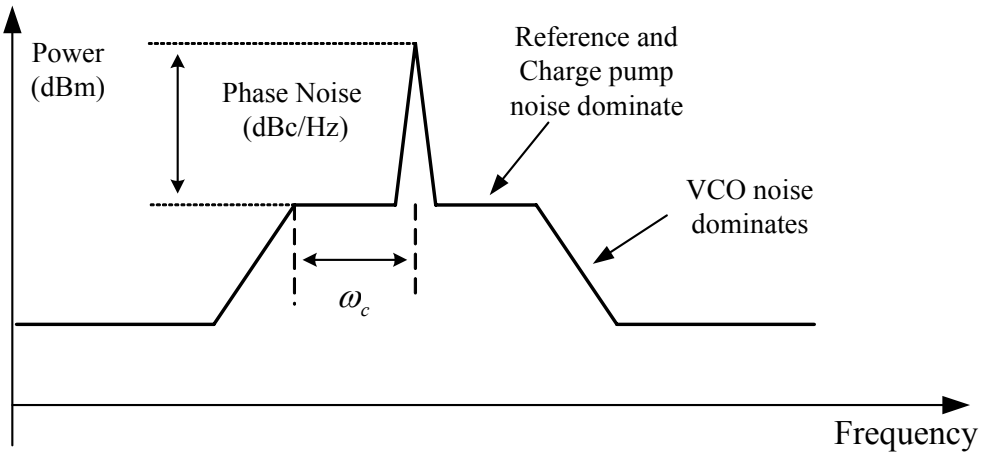


Fig. 3.9 Typical phase noise output spectrum of a PLL

From Equation (3.2), the approximate RMS phase error can be calculated as

$$RMSnoise = \frac{180}{\pi} \cdot 10^{K/20} \sqrt{2 f_c + 2} \tag{3.35}$$

where K denotes the in-band phase noise in the unit of dBc/Hz.

As expressed by Equation (3.35), the RMS phase noise decreases as the loop bandwidth of the PLL reduces. Whereas, from Equations (3.17) to (3.21), the area of the loop filter is inverse proportional to the square of the loop bandwidth. Too small a bandwidth may once again lead to an undesirable large area, which is not suitable for a monolithic design. To achieve a RMS phase noise of around 3.5 degree with an achievable in-band phase noise of K=-80 dBc/Hz, the corresponding loop bandwidth is computed to be around 137 KHz. As a trade-off result between performance and area, loop bandwidth of 120 KHz is designed. Table 3.1 summarizes the designed parameters of the PLL.

Table 3.1 Summary of the PLL parameters

Parameters	Value
Kvco	2*pi*360M/V
B	30
Icp	3.4 uA
Division Ratio	128
PNvco	-110 dBc/Hz @1MHz
Loop Bandwidth	2*pi*120KHz
Phase Margin	60
R1	2.4868 K
C1	68.909 pF
C2	62.795 pF
R3	2.4868 K
C3	68.909 pF

The open loop gain and phase response of the PLL is shown in Fig. 3.10; the loop system is designed to have a maximum phase margin of 60 degree at the loop bandwidth point. Fig. 3.11 plots the noise transfer function of each building block together with the total phase noise plot for the whole PLL.

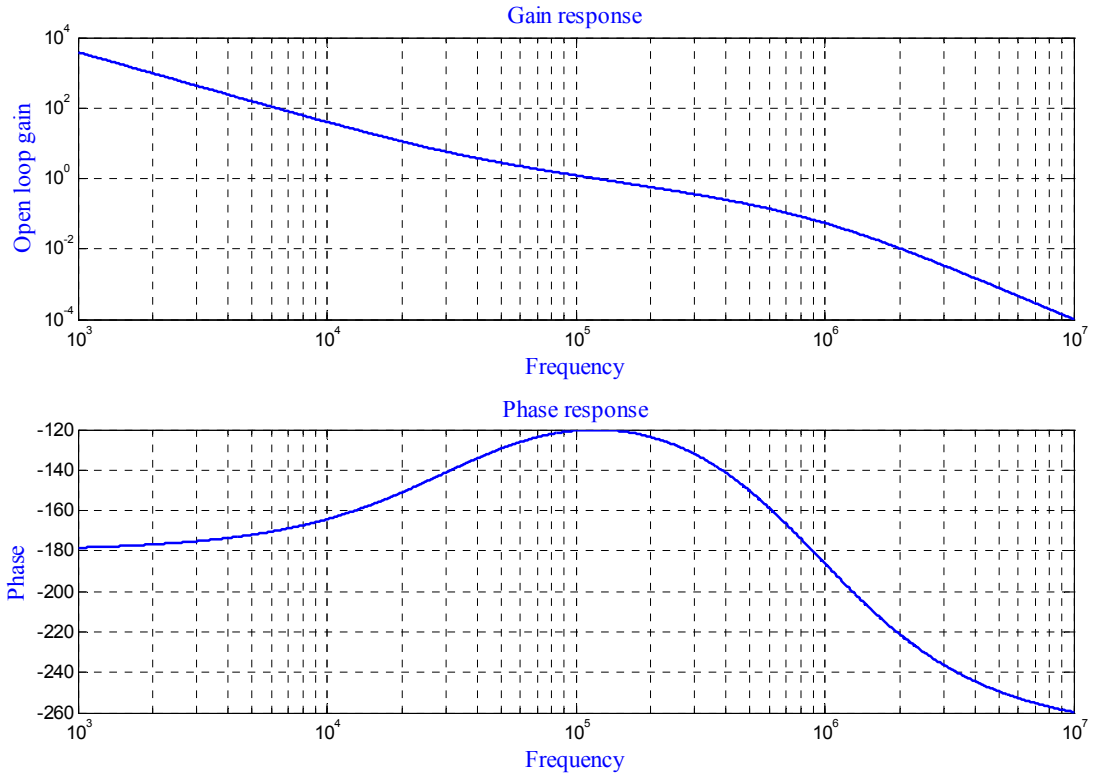


Fig. 3.10 Open-loop gain and phase response

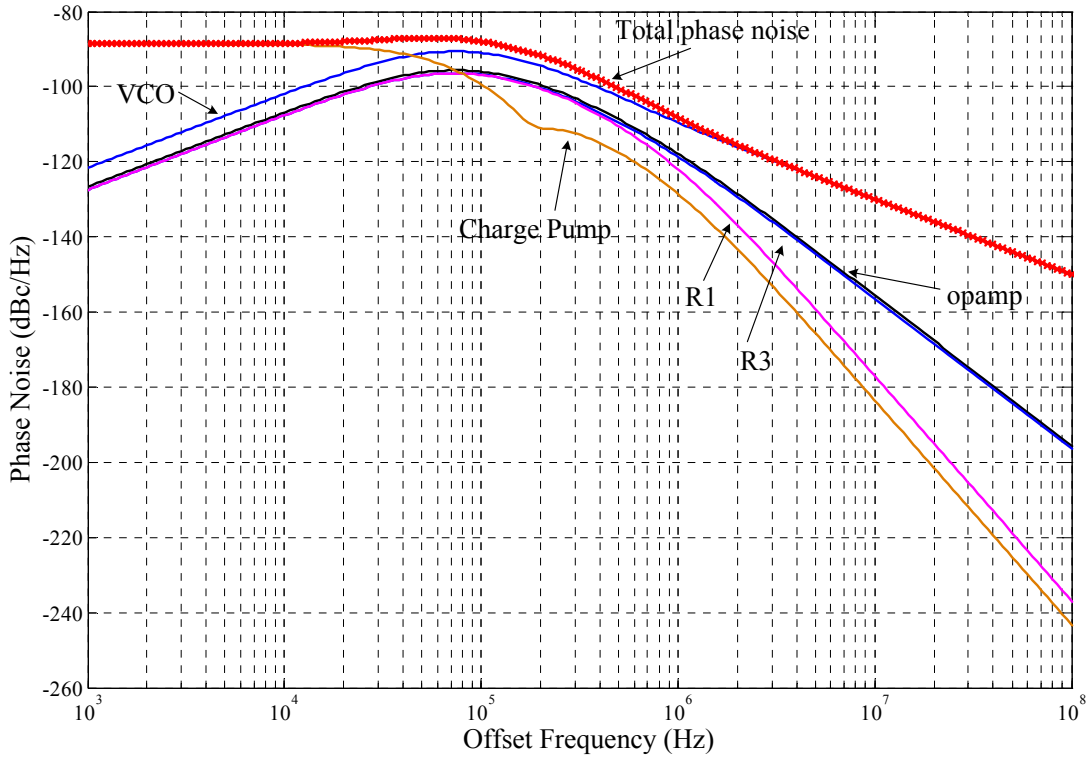


Fig. 3.11 Calculated phase noise plot

3.4.3 Phase-Frequency Detector (PFD)

The schematic of the PFD is shown in Fig. 3.12, which consists of two D-flip-flop with simplified function and NOR gate in the feedback path for reset. The DFF output goes to Low on a rising clock edge as long as the “reset” is low. The output remains Low until the “reset” input is high. The operation principle of the PFD is illustrated in Fig. 3.13.

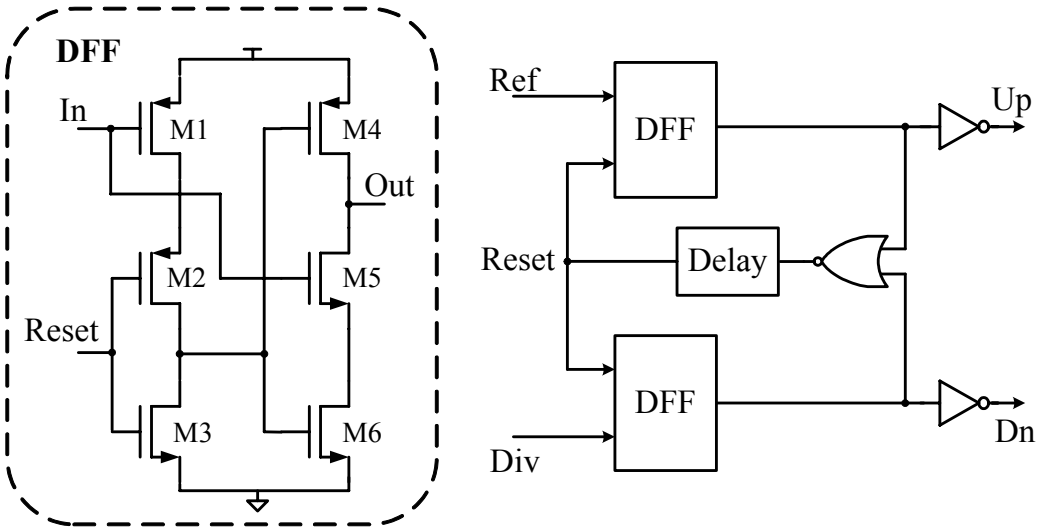


Fig. 3.12 Schematic of the phase-frequency detector

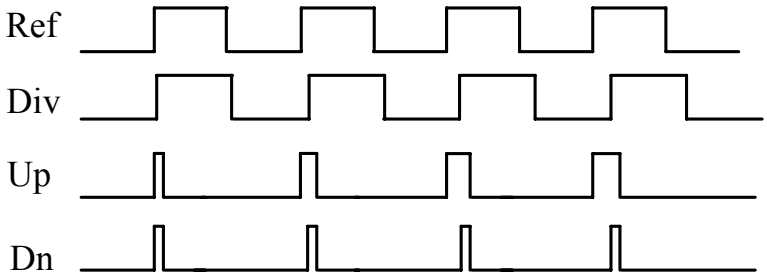


Fig. 3.13 PFD operation

The most important problem of the PFD is the “dead zone” phenomenon. If both the reference and the divider pulse appear at the same time, none of the outputs becomes active. Even if the phase difference changes slightly, the PFD will not immediately respond to this since it requires some of the finite time for the Up and Dn pulses to propagate through the circuit. However, this problem can be remedied by giving a fixed minimum width to both the pump pulses. As shown in Fig. 3.12, a delay circuit is implemented in the feedback path to introduce the minimum pulse of around 1~2 ns in width.

3.4.4 Charge Pump

The schematic of the charge pump is illustrated in Fig. 3.14. To prevent the

voltage rippling at nodes A and B, a dummy branch M1~4 is added. Once the switches M5~8 are turned off, the switches M1~4 are turned on simultaneously. Consequently, it avoids charge and discharge happening at Nodes A and B. Moreover, the output DC reference voltage at dummy branch is positioned as Vref, which is forced to the same level as the voltage at loop opamp input. Such that, when the PLL is locked, both active branch and dummy branch have the same output DC voltage of Vref. Likewise, better matched Up and Down currents in the charge pump can be achieved.

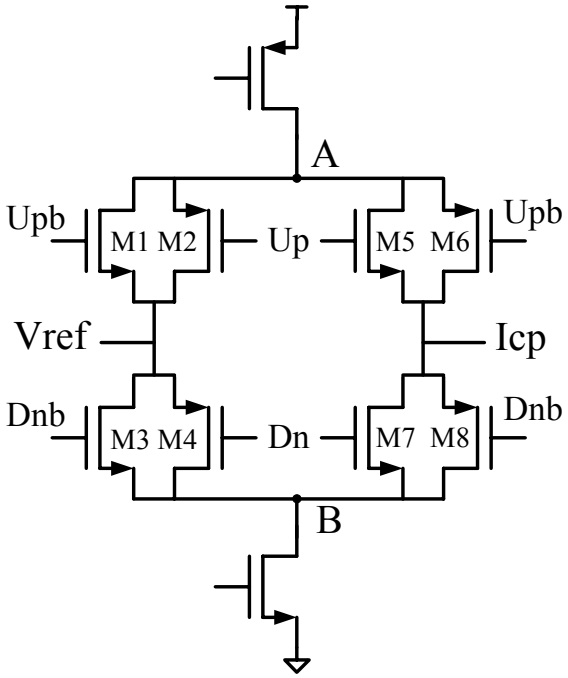


Fig. 3.14 Schematic of the charge pump

3.4.5 Loop Opamp

In the aforementioned loop filter transfer function expressed in Equation (3.8), an ideal opamp with infinite gain and bandwidth is assumed. Nevertheless, the practical opamp will have finite gain and unit gain bandwidth. Assume that the opamp transfer function is represented by A(s), consequently, the loop filter transfer

function is modified as

$$Z_A(s) = \frac{A(s)}{1 + A(s)} Z(s) \tag{3.36}$$

Eq. (3.36) implies that the loop system requires a unit gain bandwidth of the opamp to be larger than the loop bandwidth. Thus, a simple two-stage topology is enough, which is shown in Fig. 3.15.

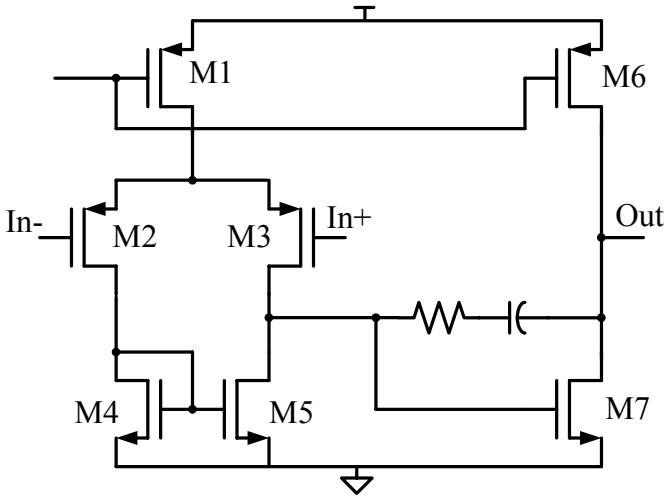
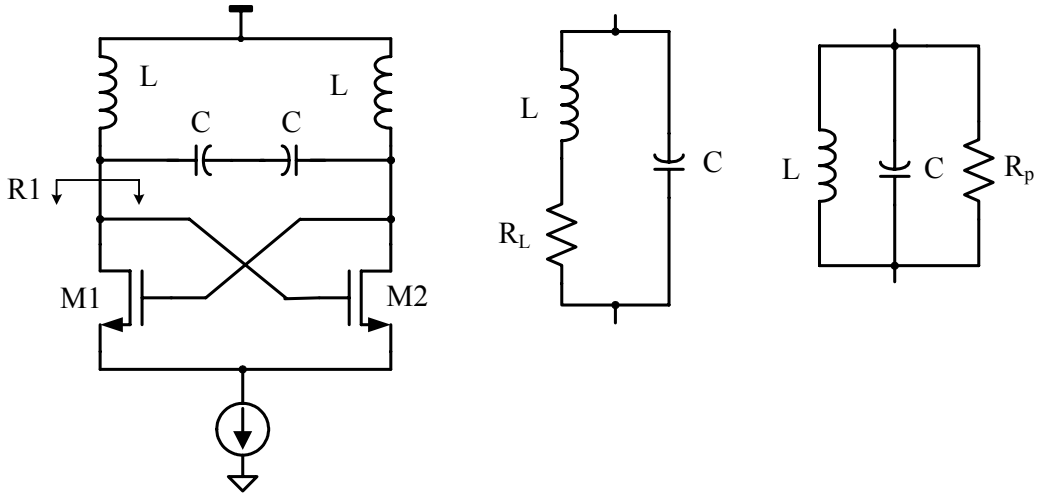


Fig. 3.15 Schematic of the loop opamp

3.5 Quadrature VCO

3.5.1 VCO Fundamentals

In modern RF oscillators, LC-VCO is a good candidate to achieve an oscillation at higher frequency with lower phase noise and lower power consumption. As shown in Fig. 3.16, the LC-VCO consists of two LC-tank resonators and two cross-coupled active devices.



(a) (b) (c)

Fig. 3.16 Schematic of the (a) LC-VCO, (b) LC-tank resonator, and (c) equivalent circuit of (b)

There are two popular models, one-port model and two-port model, which can be used to analyze the operation of the VCO. In the one-port model, the oscillator is treated as two one-port networks connected to each other. The LC-tank resonator itself does not oscillate due to the loss in the tank modeled by resistor R_p. The idea in the one-port model is that the cross-coupled transistors M1 and M2 generate a negative impedance of – 1/gm that is equal to R_p to eliminate the loss. In essence, the energy lost in R_p is compensated by the cross-coupled active devices, allowing steady oscillation.

In the two-port model, the LC-VCO can be viewed as a feedback circuit, as illustrated in Fig. 3.17. For steady oscillation, two conditions must be simultaneously met at the oscillation frequency ω_0: (1) the closed-loop gain at ω_0 must be equal to unity, or the open-loop gain at ω_0 is larger than one, and (2) the total phase shift around the loop must be equal to zero. Note that, an oscillatory system satisfying the

above conditions, however, will only sustain the steady oscillation at the frequency point where the VCO can have the maximum output amplitude. Obviously, this happens at the peak of the LC-tank in the LC-VCO shown in Fig. 3.16.

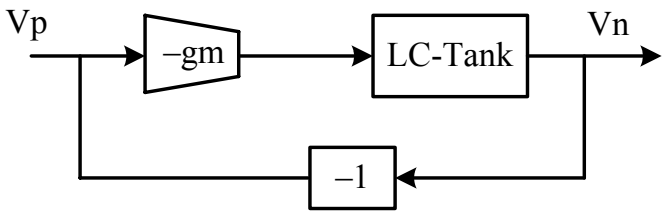


Fig. 3.17 Feedback model of the LC-VCO

3.5.2 Transformer-Feedback VCOs

VCOs are always an attractive research topic so that engineers put a lot of effort into developing various types of architectures with high performance. Recently, a transformer-feedback VCO (TF-VCO) has been reported in [7] for low voltage and high performance operations. As shown in Fig. 3.18 (a), the TF-VCO employs an integrated transformer in place of the inductor in the conventional VCOs. The transformer's primary coil with self-inductance L_d is connected at the transistor drain terminal, which forms an LC-tank with the corresponding capacitive elements. The secondary coil with self-inductance L_s is connected at the source terminal. Both the primary coil L_d and the secondary coil L_s are magnetically coupled to each other with a coupling factor K. With the transformer feedback, the drain voltage could swing above the supply voltage and the source voltage could swing below the ground potential, and most importantly, the drain and source signal oscillate in phase. Effectively, the oscillation amplitude is enhanced, and consequently, the supply voltage can be reduced for the same phase noise with lower power consumption or

for better phase noise with the same power consumption.

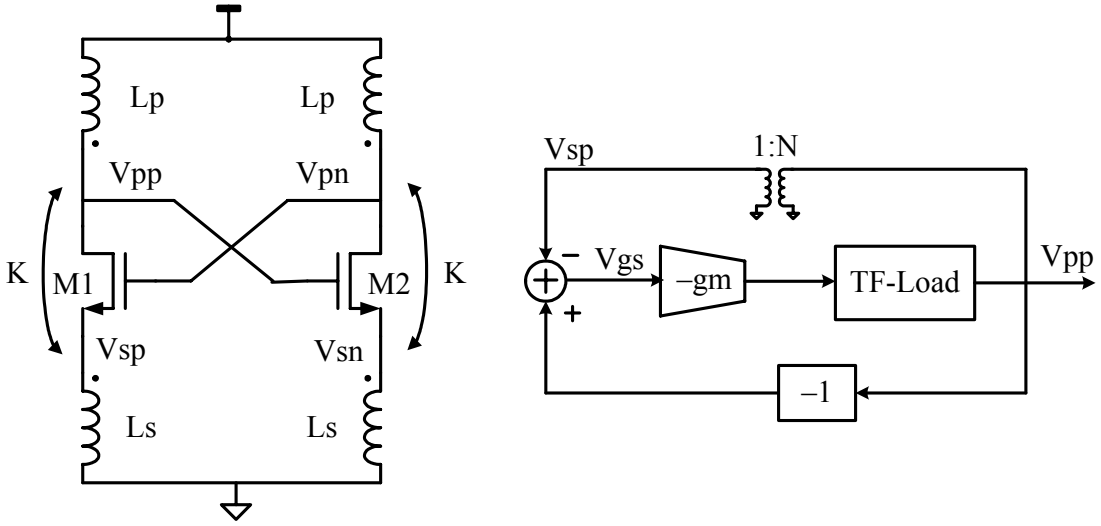


Fig. 3.18 (a) Schematic of the TF-VCO, (b) feedback model of the TF-VCO

To give additional insight into the operation, the feedback model of the TF-VCO is illustrated in Fig. 3.18 (b). Compared with the conventional VCOs shown in Fig. 3.17, the TF-VCO contains another positive feedback loop formed by transformer. Thus, the open-loop gain is enlarged, which in turn leads to the better performance.

To reduce the capacitive loading to the primary coil, a variation of the TF-VCO can be performed. Fig. 3.19 presents the schematic of the modified TF-VCO, in which the gate terminal of transistors M1 and M2 is cross-coupled and connected to source terminal of the devices instead of the drain terminal. With such variation, the gate capacitance is switched to second coil of the transformer. The capacitive loading seen from primary coil is hence reduced by the transformer ratio. Nevertheless, from the feedback model shown in Fig. 3.19 (b), it can be seen that the open-loop gain of the revised TF-VCO is smaller than the original one. As a result, the power as well as the transistors size may need to be increased to compensate the open-loop gain drop.

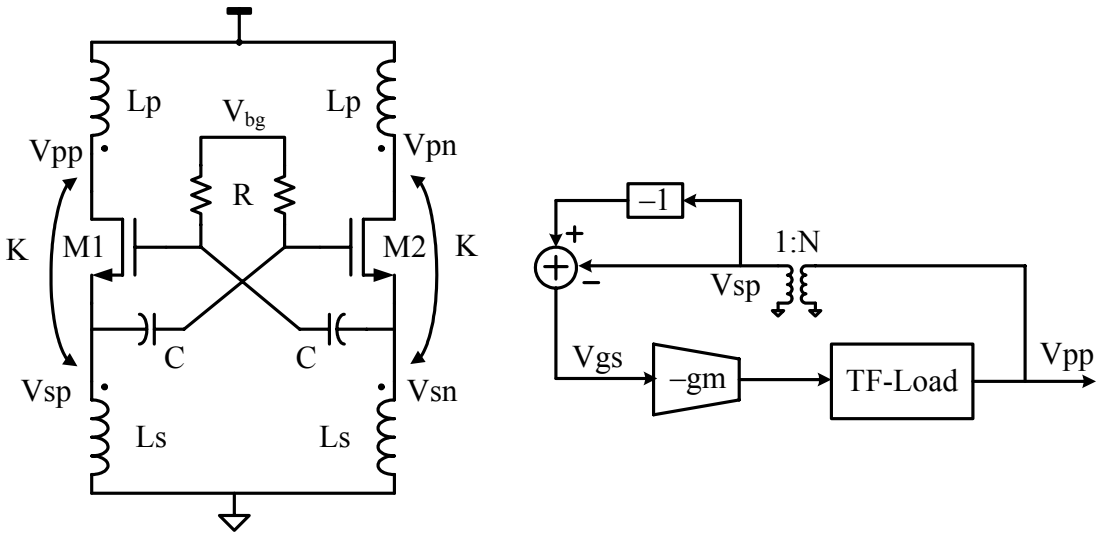


Fig. 3.19 (a) Schematic of the variation of the TF-VCO, (b) feedback model of (a)

3.5.3 Conventional QVCO Architecture and Its Modeling

Quadrature-phase clock signals are widely required in many direct-conversion or dual-conversion wireless transceiver systems for in-phase and quadrature-phase (IQ) mixing. At present, one of the popular approaches is to let a VCO works at double the desired frequency, and then to obtain quadrature signals at the desired frequency via frequency division. Another attractive way of obtaining quadrature signals is to directly use a quadrature VCO (QVCO) constructed by two cross-coupled LC-VCOs [8] [9]. Fig. 3.20 shows one of the well-known QVCO topologies, wherein two LC-VCOs are cross-coupled each other through the parallel active transistors Ms. To gain a better understanding of the behavior, the Q-output part of the parallel coupled QVCO (PC-QVCO) is represented by the feedback loop model shown in Fig. 3.21. The quadrature cross-coupled part and the VCO part of the PC-QVCO are viewed as gms and gml in the model, respectively. To start with, the ideal quadrature outputs are assumed. Furthermore, both $+\pi/2$ and $-\pi/2$ phase shift cases are modeled in Loop 2 to cover two scenarios due to the ambiguity of the

quadrature output phase sequence.

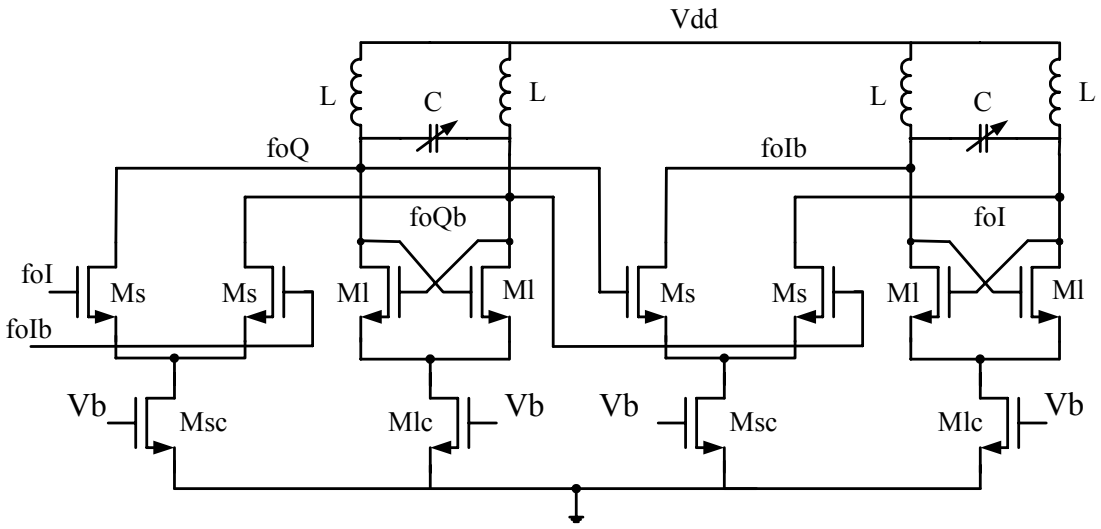


Fig. 3.20 Schematic of the conventional QVCO

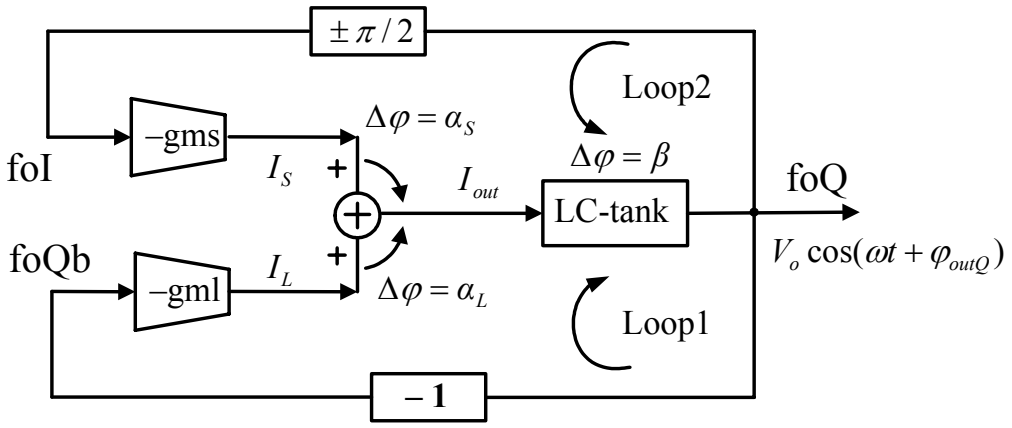


Fig. 3.21 Feedback loop model for Q-output part of the PC-QVCO

From the aforementioned two conditions for an oscillator to sustain oscillation, the phase shift around Loop 1 must be zero, which results in

$$\alpha_L + \beta = 0 \tag{3.37}$$

where α_L is the phase shift induced by the current adding of I_S and I_L, and β presents the phase shift introduced by the LC-tank.

Fig. 3.22 plots the phasor diagram of the output current I_{out} in the loop for both I-output leads Q-output and I-output lags Q-output cases. This implies that there are

two possible solutions for Eq. 3.37, as expressed by

$$\beta = \pm|\alpha_L| \tag{3.38}$$

The α_L, here, is derived as

$$|\alpha_L| = \arctan\left(I_S \big/ I_L\right) = \arctan\left(gm_S \big/ gm_L\right) \tag{3.39}$$

As a consequence, we have

$$\beta = \pm\arctan\left(gm_S \big/ gm_L\right) \tag{3.40}$$

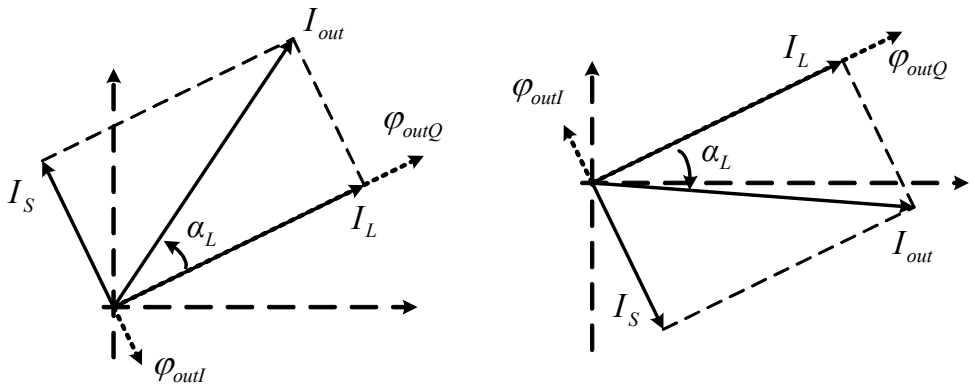


Fig. 3.22 Phasor diagram of the output current

On the other hand, the impedance of the LC-tank shown in Fig. 3.23 can be calculated by

$$Z = \sqrt{\frac{L}{C}} \frac{1 + j\,\omega/\omega_0\, Q}{Q\left[1 - \left(\omega/\omega_0\right)^2\right] + j\,\omega/\omega_0} \tag{3.41}$$

with $Q = \dfrac{\sqrt{L/C}}{R}$ and $\omega_0 = \dfrac{1}{\sqrt{LC}}$

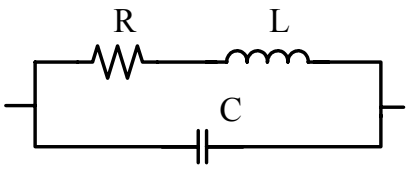


Fig. 3.23 Schematic of the LC-tank

Likewise, the magnitude and the phase of the LC-tank are plotted in Fig. 3.24 (Q=5)

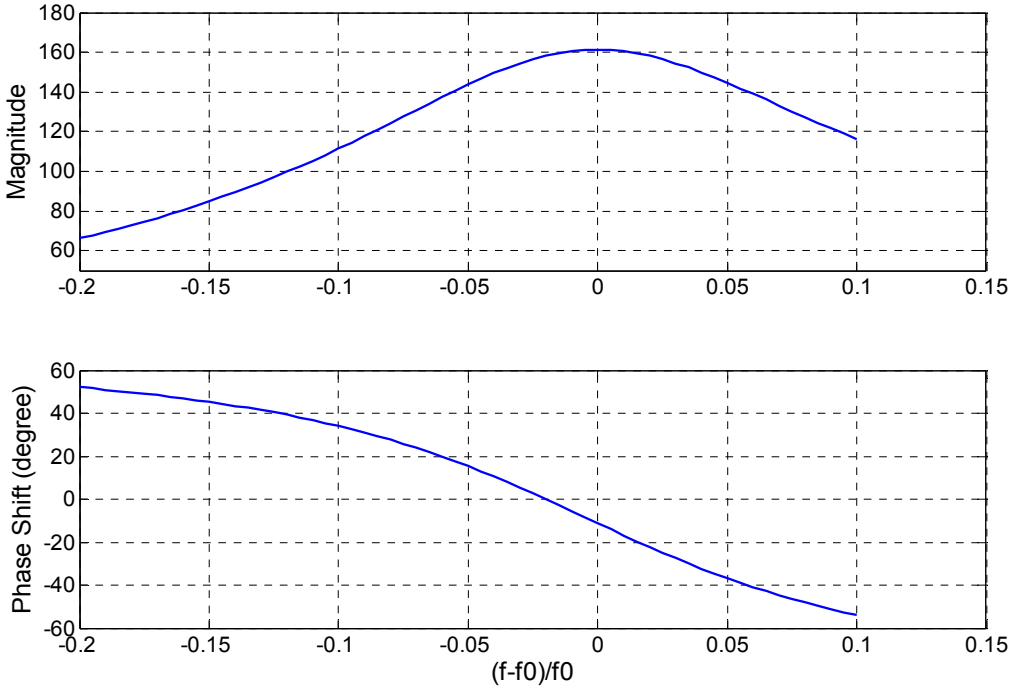


Fig. 3.24 Magnitude and phase plots of the LC-tank

Fig. 3.24 indicates an asymmetrical impedance for the same magnitude of the phase shift: the impedance at the negative phase shift is higher than that at the positive phase. Because a higher impedance results in a higher loop gain, only one solution, $\beta = -\arctan\left(gm_S / gm_L\right)$, is possible in most of the practical designs. That means the QVCO is preferable to oscillate at the frequency that is higher than the center frequency of the LC-tank, and shows an output IQ phase sequence of Q-output leads I-output.

Due to the process variations and asymmetries in the layout, a mismatch between the IQ VCOs is expected, resulting in deviations from perfect quadrature phase. To further study the IQ phase mismatch, the PC-QVCO is remodeled as the feedback loops containing both I and Q parts, which is illustrated in Fig. 3.25.

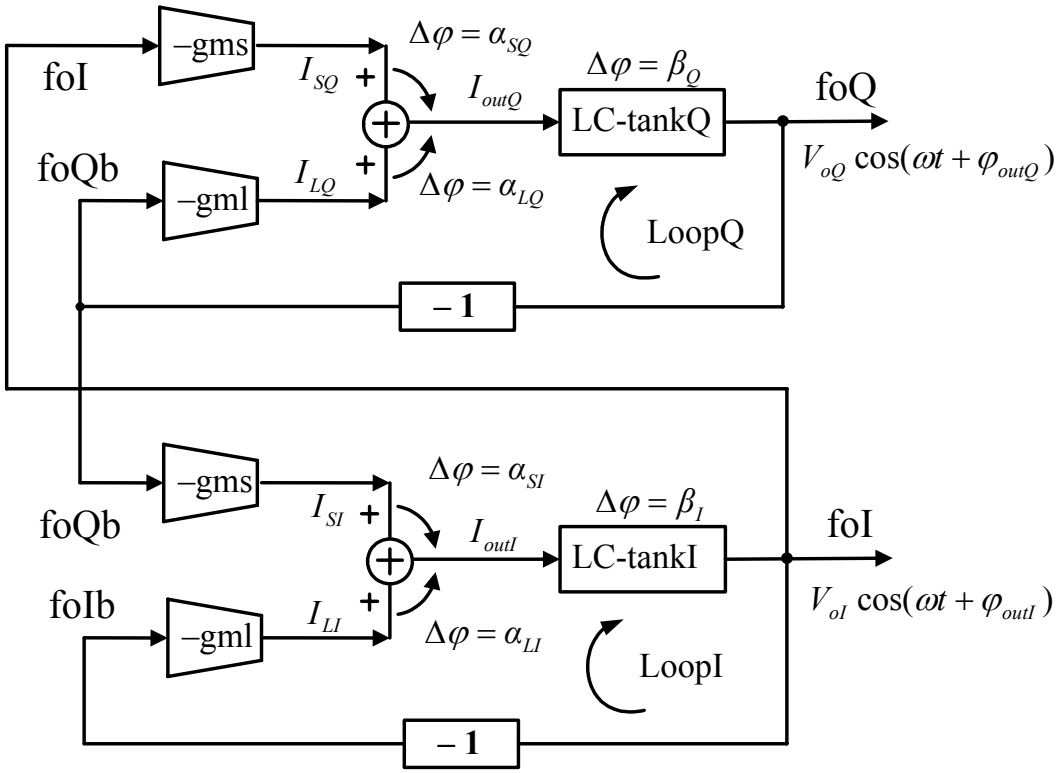


Fig. 3.25 Full model of the PC-QVCO

One of the dominated contributions to the phase error comes from mismatches in the LC-tanks, which could be caused either by capacitive mismatch or by inductive mismatch. The LC-tanks mismatches, in turn, lead to the phase shift mismatch at IQ LC-tanks for a certain frequency, as expressed by

$$\beta_Q = \beta_I - \theta \tag{3.42}$$

Similarly, we can assume the IQ outputs deviate a phase of λ from 90^o, that is

$$\varphi_{outQ} = \varphi_{outI} + \pi/2 - \lambda \tag{3.43}$$

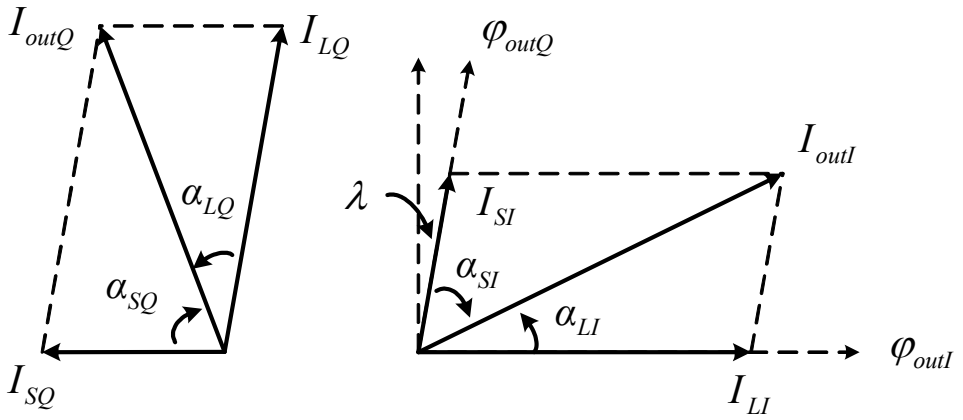


Fig. 3.26 Phasor diagram both for Q & I currents

Fig. 3.26 plots the phasor diagram of the Q-output and I-output currents in the Loop Q and the Loop I, respectively. The relevant currents can be expressed by

$$I_{LI} = g_{mL}V_{oI},\ \ I_{SI} = \eta g_{mL}V_{oQ},\ \ I_{LQ} = g_{mL}V_{oQ},\ \ I_{SQ} = \eta g_{mL}V_{oI} \tag{3.44}$$

where η is the ratio of the cross-coupled part to the VCO part, as represented by

$$\eta = g_{mS} \Big/ g_{mL} \tag{3.45}$$

By assuming the LC-tank impedances of Z_I and Z_Q, the output voltage can be calculated by

$$V_{oI} = I_{outI}Z_I,\ \ V_{oQ} = I_{outQ}Z_Q \tag{3.46}$$

With some simple calculations, the phase shifts α_{LI} and α_{LQ} can be derived as

$$\alpha_{LI} = \arccos\left(\frac{I_{LI} + I_{SI}\sin\lambda}{I_{outI}}\right) \tag{3.47}$$

$$\alpha_{LQ} = \arccos\left(\frac{I_{LQ} - I_{SQ}\sin\lambda}{I_{outQ}}\right) \tag{3.48}$$

From Eqs. (3.44) to (3.48), Eqs. (3.47) and (3.48) can be rewritten as

$$\alpha_{LI} = \arccos\left(g_{mL}Z_I(1 + \eta\frac{V_{oQ}}{V_{oI}}\sin\lambda)\right) \tag{3.49}$$

$$\alpha_{LQ} = \arccos\left(g_{mL} Z_Q (1 - \eta \frac{V_{oI}}{V_{oQ}} \sin\lambda) \right) \tag{3.50}$$

Remember that, under operation condition, the total phase shift around Loop I and Loop Q must be zero, as a consequence, we have

$$\alpha_{LQ} + \beta_Q = 0 \quad , \quad \alpha_{LI} + \beta_I = 0 \tag{3.51}$$

Thus

$$\alpha_{LQ} - \alpha_{LI} = \theta \tag{3.52}$$

From Eqs. (3.49) to (3.52), we can conclude that when θ=0, λ=0. That means an ideal QVCO without mismatch can generate perfect quadrature outputs. On the other hand, the IQ mismatch (λ) in practical QVCO can be improved by increasing the strength of the cross-coupled part (η).

3.5.4 8.5 GHz QVCO for UWB

Recently, a transformer-coupled QVCO has been proposed in [10]. Two LC VCOs are cross-coupled by on-chip transformers to generate quadrature signals. The primary coil Lp of each transformer is connected to the drain node of each VCO to resonate with the total output capacitance while being simultaneously cross-coupled to its secondary coil Ls connected at the source node of the other VCO. As such, the loading capacitors contributed by the coupling transistors are removed, and the supply voltage can be lower because the transformer enables the signals at the sources to swing below the ground. However, the quadrature accuracy of output signals is highly dependent on the magnetic coupling of the on-chip transformers.

To alleviate this problem, an active cross-coupled loop is added to the transformer-coupling QVCO to enhance the cross-coupled strength. Fig. 3.27 shows

the detailed schematic of the proposed QVCO. A top-biased PMOS current source is used to provide the required DC output voltage for the following dividers and WB-SSB mixer stages. Thus, the AC coupling capacitors between VCO and later stages can be avoided, which are required in bottom-biased VCO. To reduce the up-conversion of 1/f noise and reduce the VCO gain at the same time, fixed capacitors are added in series with the varactors, and bias resistors R are used to provide the dc voltage for the internal nodes.

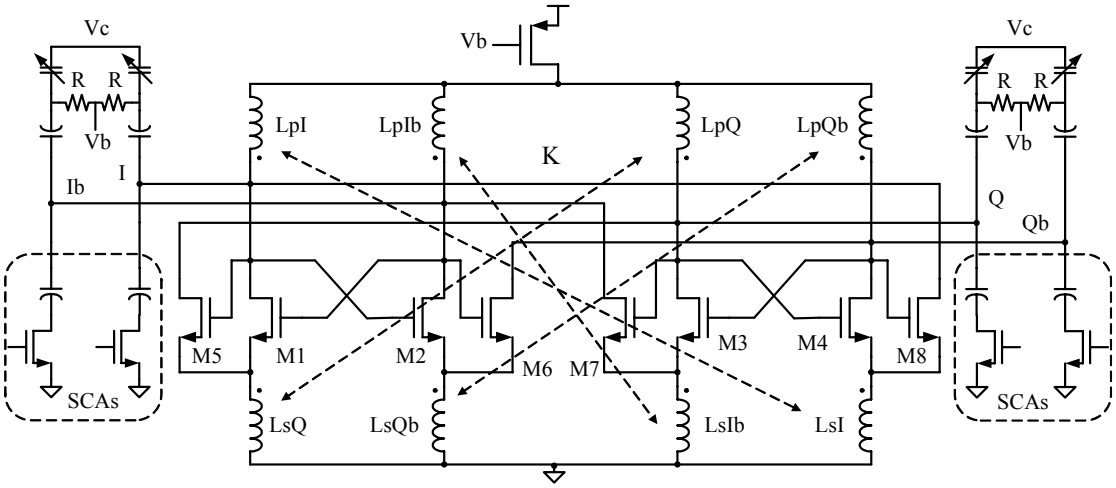


Fig. 3.27 Schematic of the proposed QVCO

To fully understand the operation, the active cross-coupled loop (ACCL) is decomposed from the QVCO, which is shown in Fig. 3.28. Note that the proposed QVCO consists of the ACCL and the transformer-coupled QVCO proposed in [10]. As explained in Fig. 3.28, the ACCL provides the additional quadrature loop gain to the QVCO, which is formed by 4 common-source amplifiers (M5~M8) connected in series. In addition, the ACCL also contributes part of the feedback gain or negative gm to the VCO, which is constructed by the transformer Lp, Ls and transistors working in common-gate amplifier mode.

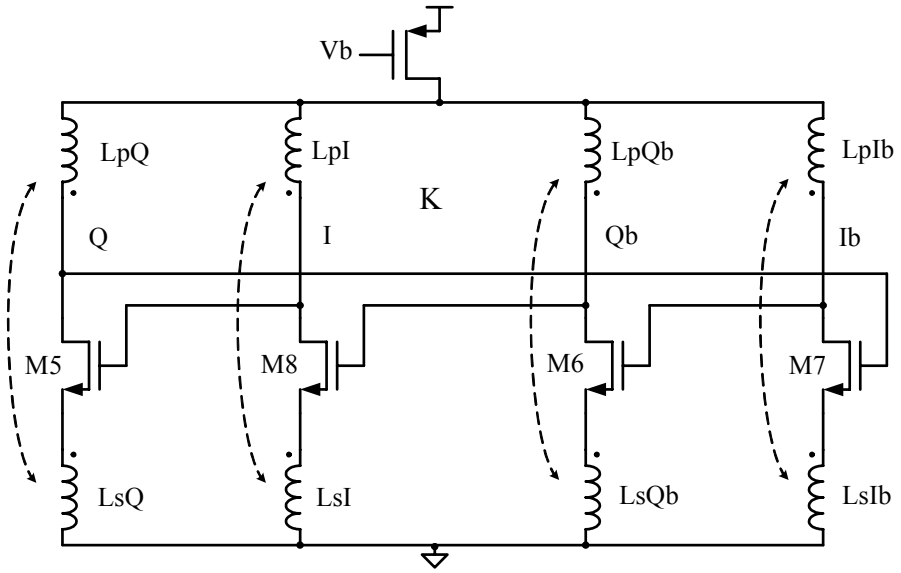


Fig. 3.28 Schematic of active cross-coupled loop in the QVCO

3.6 Frequency and IQ Phase Multiplexers

In order to accomplish the band switching within few nanoseconds, high frequency multiplexer (MUX) circuits are implemented both for frequency and IQ phase switching. As shown in Fig. 3.29, the IQ phase MUX is constructed by two differential pairs sharing the same resistor loads. The coming signals are controlled by transmission gates M6~7, and disable transistors M5 are added from the gates of the differential pair transistors to ground. When signal 1 is selected, the switches S1 and S2 are settled to on and off respectively, the differential pair transistors M2~3 are shut down by transistor M5. Therefore, good isolation is achieved between different inputs. At DC mixing case, both switches S1 and S2 are turned off, so that all transistors M1~4 are disabled. The same design is applied to frequency MUX, and four differential pairs are required for four frequency selection.

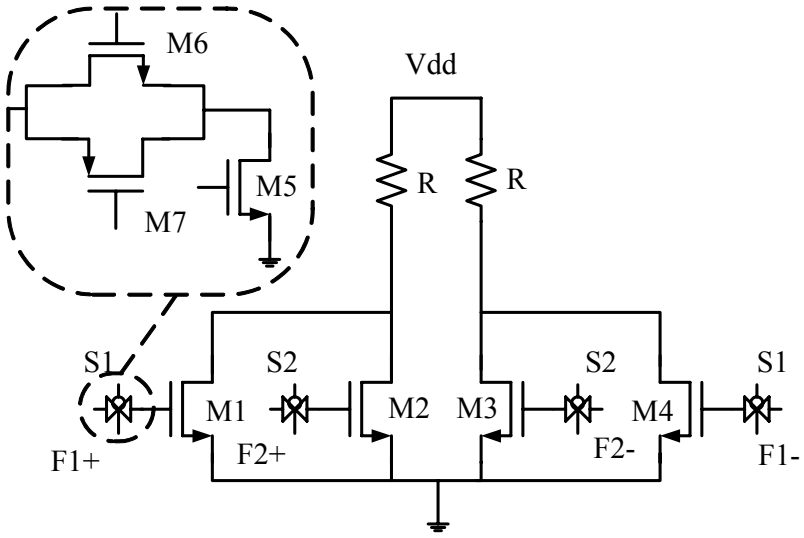


Fig. 3.29 Schematic of the proposed high-frequency MUX

3.7 Single-Sideband Mixer

As shown in Fig. 3.5, two SSB mixers are needed to generate the internal frequencies. The classical Gilbert cell mixer is chosen, as shown in Fig. 3.30. The output current of the two mixers are added together, thereby either up-sideband or lower-sideband can be suppressed, which depends on the phase polarity between two input frequencies. The tail current of the two mixers are removed for low voltage operation. Combined with the narrow band characteristic of the LC Tank, good sideband suppression can be achieved.

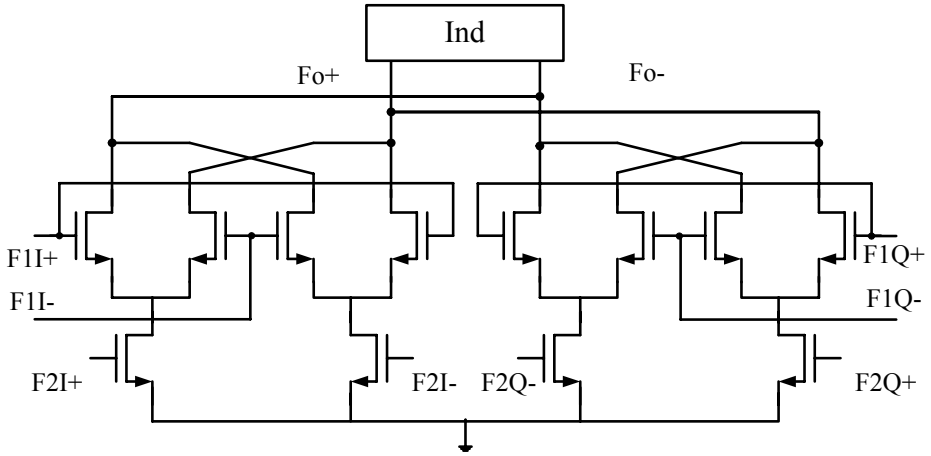


Fig. 3.30 Schematic of the adopted SSB Mixer

3.8 WB-SSB Mixer with Proposed Wideband Inductive Network

3.8.1 Design Considerations

To generate the 1st LO from 6.336 GHz to 10.56 GHz in our proposed UWB synthesizer, a high frequency wideband load is required for the WB-SSB Mixer. In narrowband RF circuits, parallel resonant LC structures are widely used as loads. In low-cost CMOS processes, the maximum Q achievable is dominated by the on-chip inductor Q and is limited to around 5 to 8. As a result, a limited bandwidth of less than 1GHz is obtained for center frequencies around 8 GHz, which is not enough for this wideband application [11]. A simple method to increase the bandwidth is to decrease the Q of the tank, but this is undesirable in terms of the gain and the power consumption. An alternative way to increase the bandwidth is to tune the tank's resonant frequency depending on the desired channel.

For LC tanks, the center frequency can be tuned either by L or C. The most commonly used mechanism is to vary the parallel capacitors either by varactors or switched-capacitor arrays (SCAs). However, only up to 30~40 % tuning range can be observed at such high frequency, which can not meet the more than 50 % tuning range requirement for this application. On the other hand, since the tank impedance would be degraded with the increased capacitance, the tank impedance is lower at lower frequencies as compared to that at higher frequencies. Consequently, either the output swing or the power consumption would need to be compromised. As a better alternative to vary the parallel capacitors, entirely separate tank circuits for different frequencies can be switched effectively. However, the most obvious problem with

this approach is that multiple output nodes exist for different tanks.

Of course, there are other kinds of wideband technologies, such as inductive peaking and T-coil and so on [12]. Whereas, these technologies typically are suitable for the applications in which a bandwidth from DC to certain frequency is needed.

3.8.2 Proposed Wideband Inductive Network

To address aforementioned problems, an integrated wideband inductive-network is proposed using an on-chip transformer L1 and L2 together with two switched series LC branches as shown in Fig. 3.31.

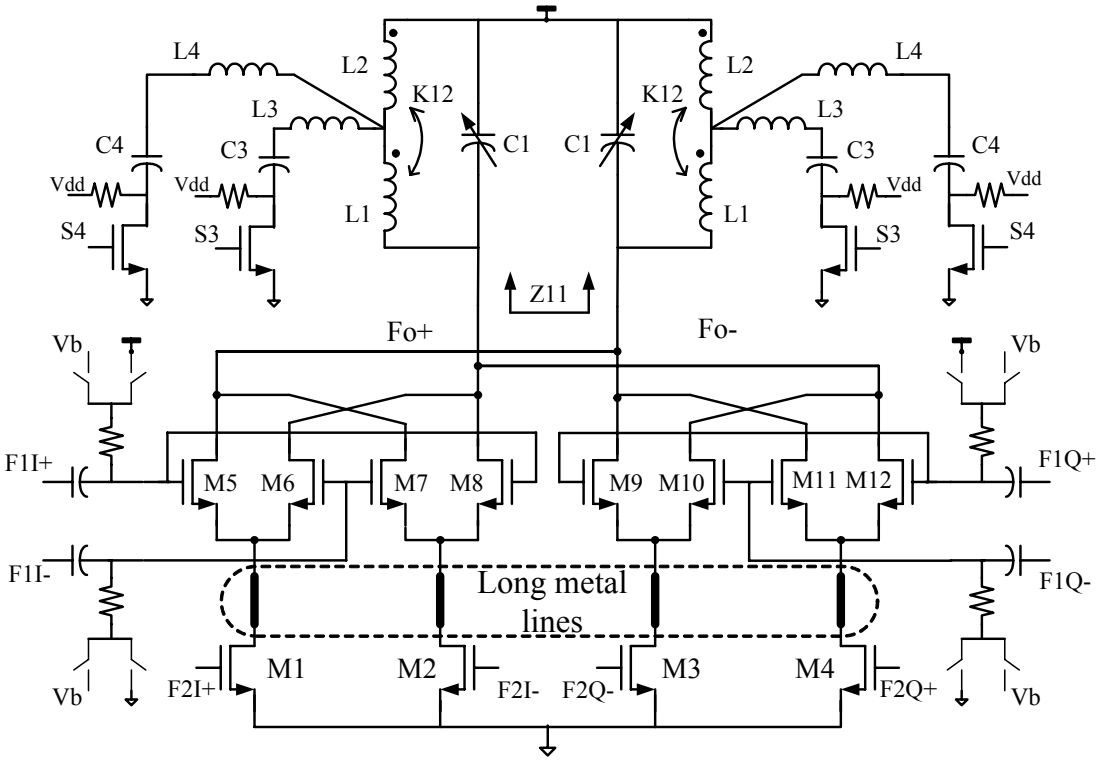


Fig. 3.31 Schematic of the WB-SSB mixer with the proposed wideband inductive network

Here, the transistors S3 and S4 only function as switch, and C1 are switched-capacitor arrays. For simplicity, the switched series LC branches can be expressed as L34 with C34, and the coupling coefficient K12 is set to be zero. Then,

the impedance Z11 can be written as follows:

$$|Z11| = \left| \frac{\left[(L_1 L_{34} + L_1 L_2 + L_2 L_{34}) C_{34} \omega^2 - (L_1 + L_2) \right] \omega}{(L_1 L_{34} + L_1 L_2 + L_2 L_{34}) C_1 C_{34} \omega^4 - (L_{34} C_{34} + L_2 C_{34} + L_1 C_1 + L_2 C_1) \omega^2 + 1} \right| \quad (3.53)$$

As expressed by the equation, two peak frequencies exist, which can be selected by switching the series LC branches. For an extreme case, C34 is close to zero (C1>>C34), which can be realized by turning off the transistors S3 and S4. In Mode 1, in which the first peak at the lower frequency has a larger impedance, LC arrays are switched off, and the inductive-network only functions as a simple parallel LC tank formed by L1, L2 and C1. At the other extreme case, when C34 is much larger than C1 (C34 >> C1), which can be achieved by tuning on S3 or S4 and minimizing C1. The impedance Equation (3.53) can be approximated as:

$$|Z11| = \left| \left(1 - \frac{(L_1 + L_2)}{(L_1 L_{34} + L_1 L_2 + L_2 L_{34}) C_{34} \omega^2} \right) \Big/ \left(C_1 \omega - \frac{L_2 + L_{34}}{(L_1 L_{34} + L_1 L_2 + L_2 L_{34}) \omega} \right) \right| \quad (3.54)$$

Therefore, the second peak at the higher frequency has a larger impedance, which is defined as Mode 2. Here, two LC arrays, L3 and L4 are included. Large capacitors C3 and C4 are employed to switch between the two modes. By turning on or off the switch transistors S3 and S4, three frequency bands at Mode 2 can be achieved with relative constant impedance as shown in Fig. 3.32. Combining with the fine tuning from C1, more than 60 % tuning range can be achieved, and that can be further extended by including more switched series LC arrays. Table 3.2 summarizes the designed parameters of the proposed wideband inductive-network load for WB-SSB mixer.

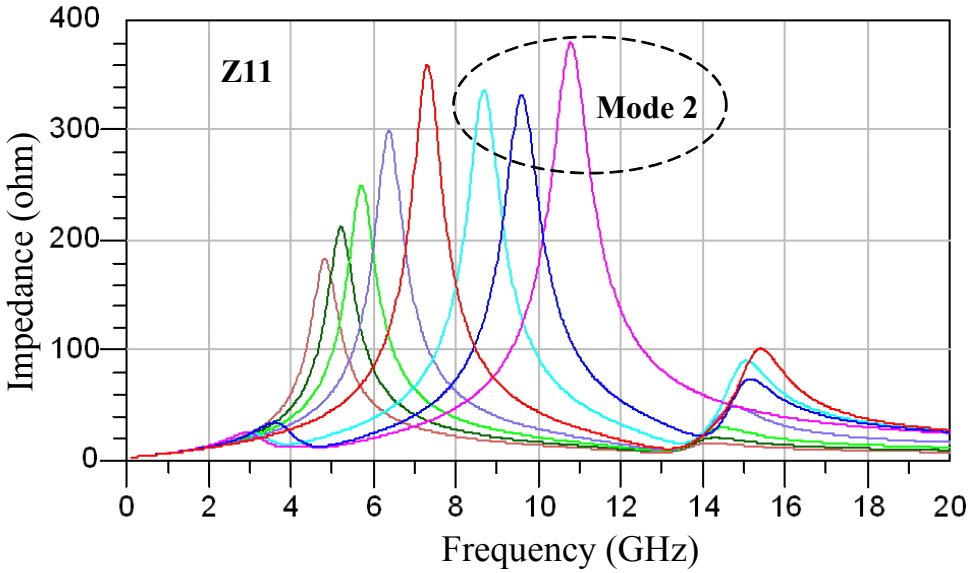


Fig. 3.32 Impedance plot of the proposed wideband inductive-network

Table 3.2 Parameters of the proposed wideband inductive-network

L1	L2	L3	L4	C3	C4
0.25n	0.25n	0.5n	0.8n	2pF	2pF

To reduce the chip area, the first core inductors L1 and L2 can be combined as transformer without sacrificing the performance. In order to minimize the off-capacitance of the switchers at Mode 1, the drain terminal of the transistors S3 and S4 are biased to Vdd through a 10K resistor to increase the reverse bias of the drain junction.

In addition, as mentioned previously, a DC mixing selection is implemented at the WB-SSB mixer stage. The DC mixing is realized by switching half of the LO transistors to ground and half to vdd, as illustrated in Fig. 3.31. In addition, the coming signals to LO terminals are disabled by previous MUX stage simultaneously; the WB-SSB mixer only works as a buffer with cascode transistors.

3.8.3 Output Impedance Measurement Results

The output impedance of the WB-SSB mixer together with the proposed wideband inductive-network is measured. As expected, as shown in Fig. 3.33, the measured center frequencies can be tuned from 6.5 GHz to 10.7 GHz with relative constant impedance, which is around 48.8 % tuning range.

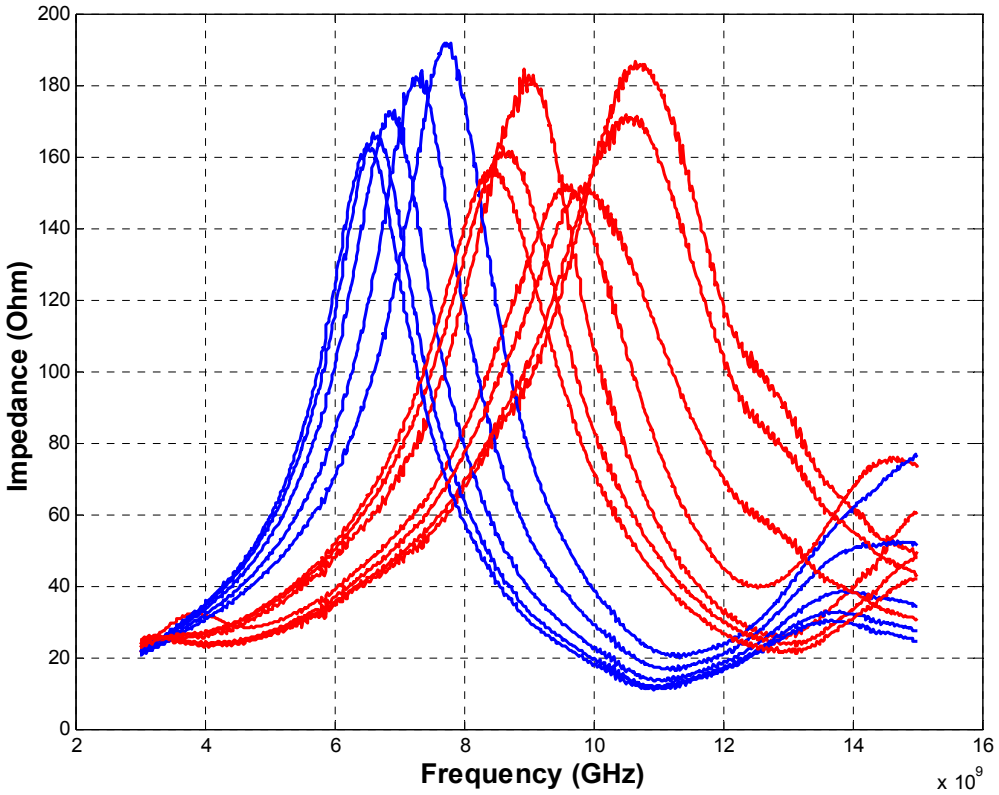


Fig. 3.33 Measured output impedance of the WB-SSB mixer

3.9 Divide-by-2 Dividers

3.9.1 First-stage Divider

The designed QVCO in the PLL is expected to deliver an accuracy quadrature phase signals to WB-SSB mixer. However, one of the critical contributions to the IQ phase mismatch of the QVCO outputs is the mismatch in its output loading, which

typically is dominated by the input capacitance of the first stage divide-by-2 circuit. To overcome this problem, a quadrature-input quadrature-output frequency divider (QIQOD) is proposed. Both the input IQ signals are utilized to achieve divided-by-2 operation, however, the phase accuracy of the input IQ signals does not affect quadrature phase accuracy of the output signals. It can reduce the capacitive load to QVCO while simultaneously achieving better IQ loading matching, wider operation range, smaller 3rd harmonics, and lower power consumption. More detailed design and analysis about the proposed QIQO divider will be addressed in Chapter 4.

3.9.2 Dynamic Loading Divider

The SSB mixers require quadrature inputs so as to perform output additions or subtractions. As illustrated in the block diagram (Fig. 3.5), many divide-by-2 dividers are required to achieve the desired quadrature signals. The current mode logic (CML) static frequency divider manifests itself in providing IQ output with high phase accuracy as shown in Fig. 3.34. The tail current of the conventional CML divider is removed for low-voltage and high-speed operation. Dynamic PMOS loading is designed to increase the operation speed by dynamically changing the output loading, which is controlled by the clkb [13]. Moreover, the transistor size ratio of the sense parts Ms and latch parts Ml is optimized to be around 4:1 to reduce the power and increase the operation speed, since they do not need to operate with wide band. In addition, they are optimized with different sizes for different frequencies requirement. For the 2nd LO divider, inductive loads are chosen for high speed operation.

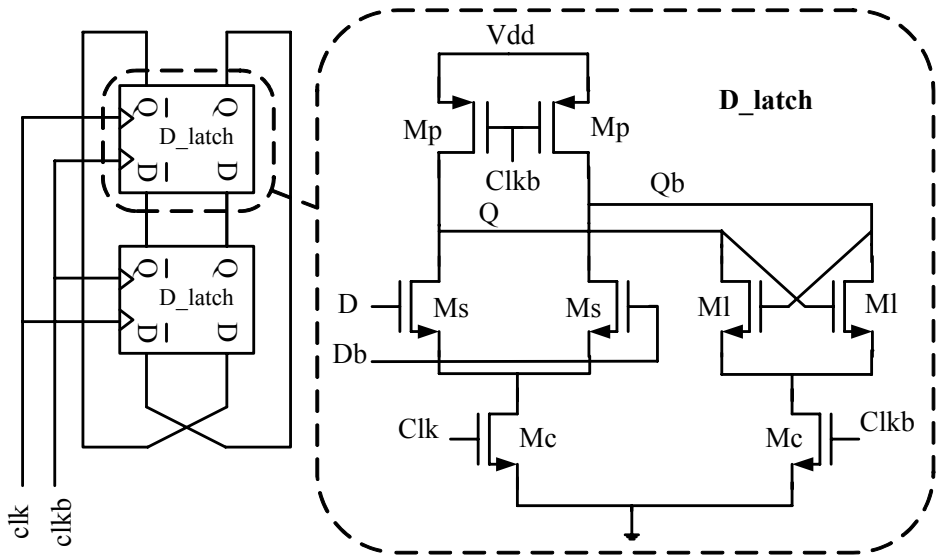


Fig. 3.34 Divide-by-2 circuit

3.9.3 Digital Divider

The last divide-by-8 stage in the PLL loop can be implemented by digital divide-by-2 circuits, since no quadrature signals are needed anymore. A static logic D-flip-flop based high frequency digital divider, as shown in Fig. 3.35, is employed for low power and glitch-free consideration. The operation of the digital divider is as follows, which consists of two steps: the transmission step and the hold step. When Finp is low, the D-flip-flop works in the hold step. The transistors PM8 and NM8, PM2 and NM2 are turned on; the value at node C is held by self-control circuitry. While, the value at node A is transmitted to node B with inverse value. When Finp is high, node B is held, node C and node A receive the value from B. Thus, divided-by-2 function is realized with operation range from DC to more than 1 GHz.

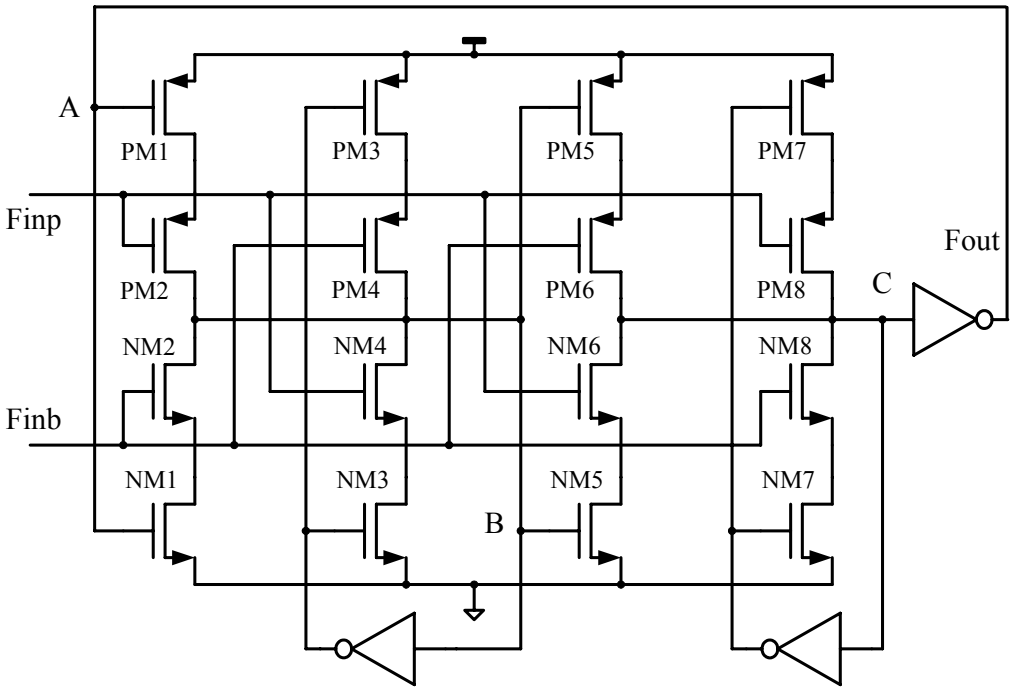


Fig. 3.35 Schematic of the digital divide-by-2 divider

3.10 Proposed Long-metal-line Loading-Insensitive Layout Technique

The on-chip inductors can not be avoided because of the high frequency application, which not only occupy large chip area but also induce the long connections between the building blocks. These long interconnection lines inevitably degrades the circuit performance in terms of frequency, gain, and power, and even may cause the circuits fail to function.

In particular, in our proposed synthesizer design, the QVCO needs to drive both the first stage divider and WB-SSB mixer at the same time, and a total of 7 center-tap inductors are needed for these three building blocks. Due to the large area introduced by the inductors, the distances from the QVCO outputs to the input devices of the 1st divider and the WB-SSB mixer are more than 700 μm and 300 μm, respectively. If they were connected directly as in conventional designs, the long interconnection

lines would introduce significant inductive and capacitive loading to the QVCO, and the QVCO would not work properly or the power would need to be increased more than double. A typical solution is to add buffers right after the QVCO outputs. However, those buffers at high frequencies not only consume large power but also occupy large chip area with more inductors.

To minimize the QVCO loading to eliminate the need for buffers, the input transistors of the 1st divider and WB-SSB mixer are moved away from their cores and laid out very closely to the QVCO output. As illustrated in Fig. 3.31, metal lines of 420 μm long are still required to connect the mixer's input transistors M1~M4 to their core; and metal lines of 130 μm metal lines are needed from the 1st divider input devices to their core. However, our proposed layout technique can significantly reduce the loading effect because the signals are operated in the current-mode domain and the long interconnections are terminated with low impedance.

3.11 Measurement Results of the Synthesizer

The proposed frequency synthesizer is designed and fabricated in TSMC 0.18-μm CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers. Fig. 3.36 shows the photograph of the chip, which occupies the area of 2.5×1.4 mm^2. Operated under a 1.8-V supply, the proposed synthesizer consumes a total current of 57mA.

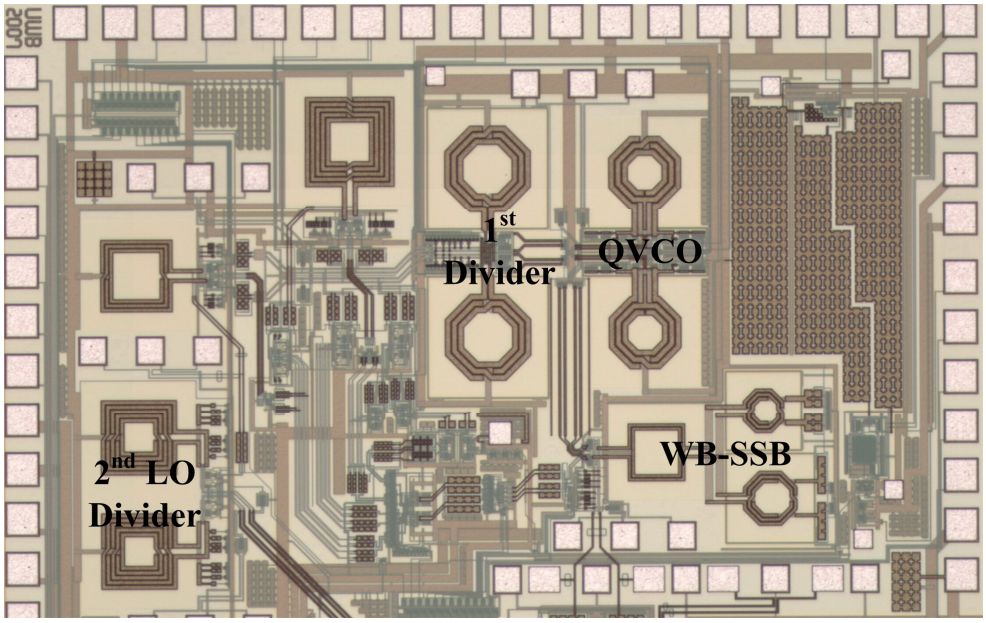


Fig. 3.36 Die photo of the proposed synthesizer

The proposed QVCO is measured with open loop measurement. Fig. 3.37 shows the measured tuning curves of the proposed QVCO. The QVCO achieves a tuning range of 16.3 %, from 8.05 GHz to 9.48 GHz, which is wide enough to compensate the process and temperature variations.

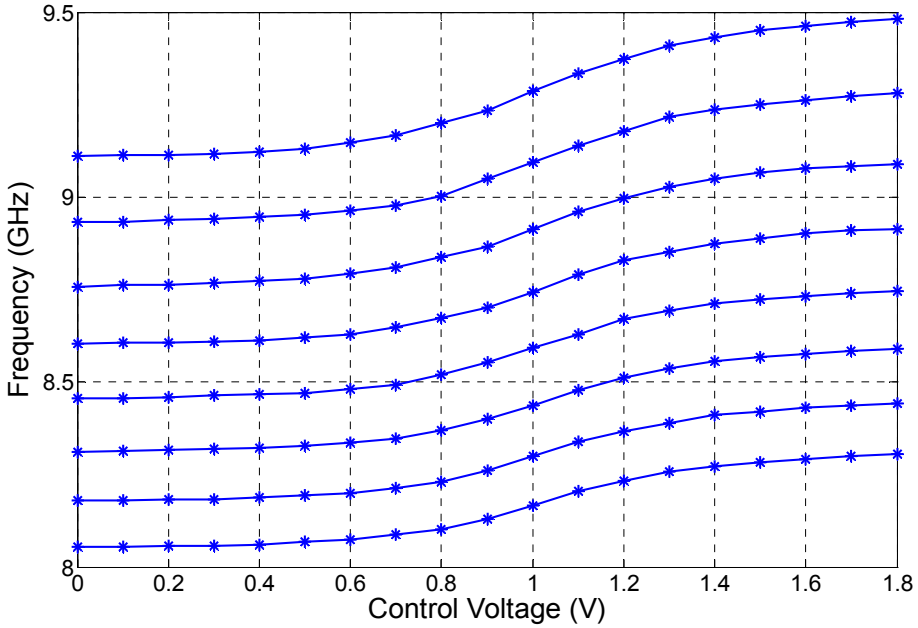


Fig. 3.37 Measured turning curves of the proposed QVCO

With an external reference of 66 MHz, the synthesizer is locked at 8.448 GHz.

As shown in Fig. 3.38, a phase noise of -130.8 dBc/Hz at 10MHz offset and an integrated phase noise of 2.88^{o} at lowest band are achieved. In contrast, the worst case integrated phase noise of 4.82^{o} is observed at 10.56 GHz band. The measured integrated phase noise actually is dominated by the phase noise of the external reference. In order to achieve in-band phase noise of better than -80dBc/Hz and an integrated phase error of smaller than 3.5^{o} for the PLL, the reference's in-band phase noise should be lower than -120dBc/Hz. Unfortunately, the best in-band phase noise for the reference generated from our Agilent E8247C signal generator is limited to around -115dBc/Hz. With a better reference either from a good crystal oscillator or from a better signal generator, the integrated phase noise can easily meet the specification.

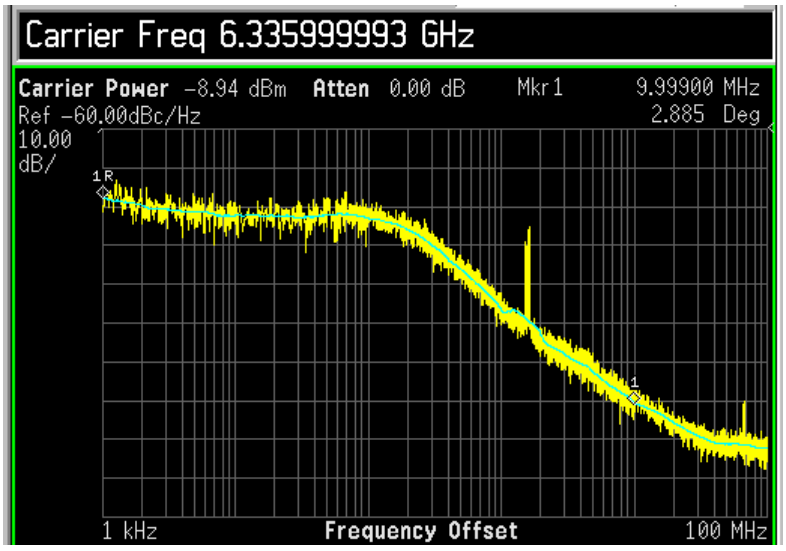


Fig. 3.38 Synthesizer phase noise plot at 6336 MHz band

The measured frequency spectrums at 6.336 GHz and 10.56 GHz band are shown in Fig. 3.39 and Fig. 3.40 respectively. The synthesizer achieves sideband rejection of better than -28 dBc for all the 9 frequency bands at 1st LO, and a better than -50 dBc harmonic suppression for the 2nd LO, as shown in Fig. 3.41.

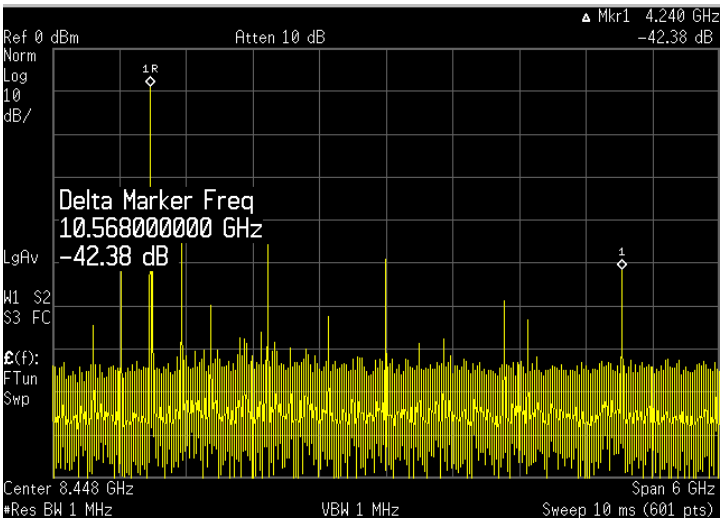


Fig. 3.39 Output spectrum of the 1st LO at 6.336 GHz band

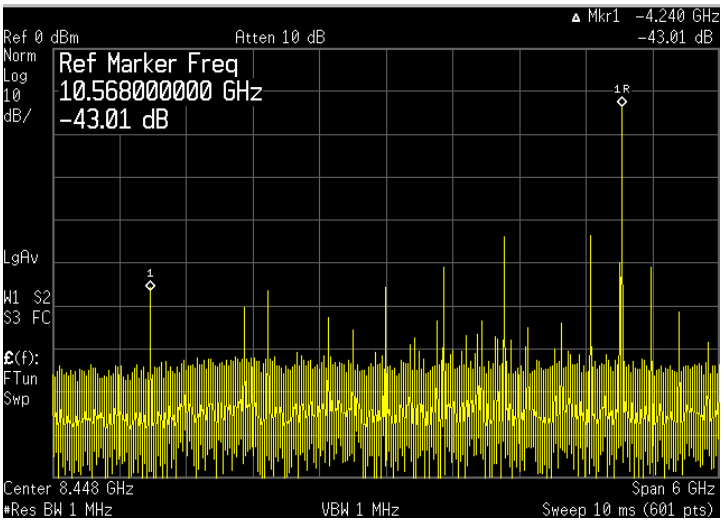


Fig. 3.40 Output spectrum of the 1st LO at 10.56 GHz band

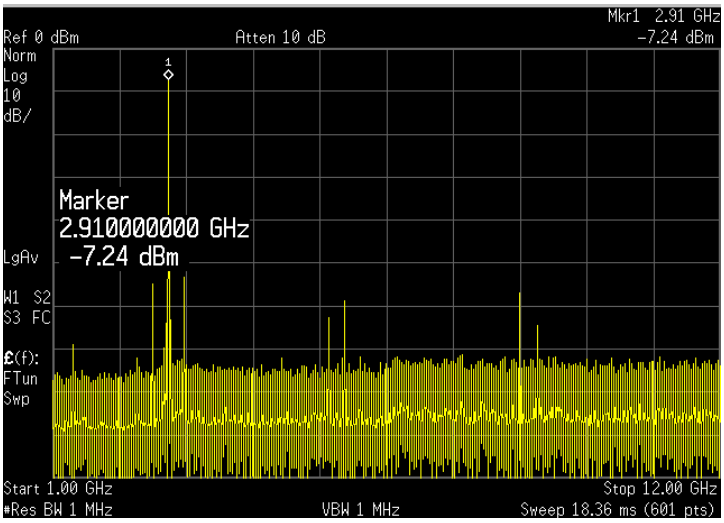


Fig. 3.41 Output spectrum of the 2nd LO

To verify the frequency band switching time, the first LO output waveform is captured in the time-domain using Agilent Infinium DCA 86100A oscilloscope. As shown in Fig. 3.42, the frequency can be switched from 6.864 GHz to 6.336 GHz band within 1ns, which is much smaller than the specification. The synthesizer can generate all the LO signals for the 9 UWB frequency bands with band switching time of less than 1ns. Single-ended output amplitude of larger than 400mVp-p is observed for all the 9 frequency bands. Table 3.3 summarizes the measured performances of the proposed synthesizer for the 9 frequency bands. Table 3.4 compares the measured performance of the proposed synthesizer with the other publications.

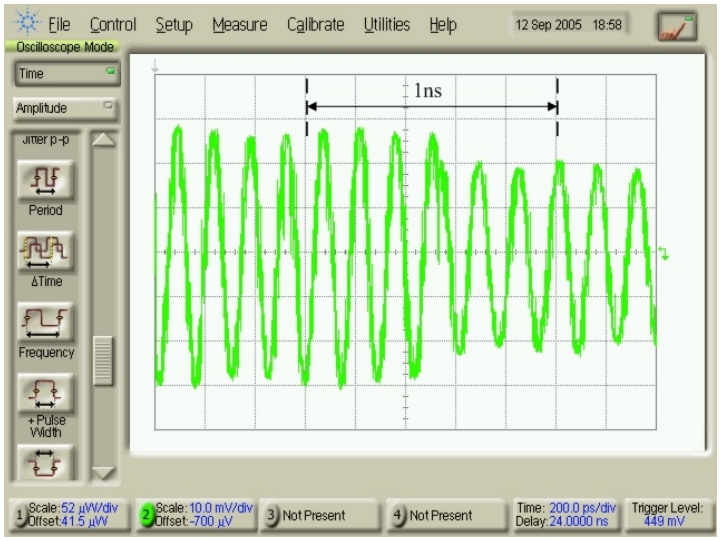


Fig. 3.42 Measured switching plot from 6.864 GHz to 6.336 GHz band

Table 3.3 Summary of the measured performances of the proposed synthesizer for 9 frequency bands

	2904 (MHz)	6336 (MHz)	6864 (MHz)	7392 (MHz)	7920 (MHz)	8448 (MHz)	8976 (MHz)	9504 (MHz)	10032 (MHz)	10560 (MHz)
Sideband suppression (dBc)	**< -50**	**-43.1**	**-45.5**	**-36.4**	**-35.3**	**< -40**	**-28.3**	**-27.9**	**-33.7**	**-43**
PN@10MHz (dBc/Hz)		**-130.8**	**-130**	**-129.7**	**-129.4**	**-128.3**	**-127.3**	**-126.7**	**-127.1**	**-127.6**
RMS Noise (degree)		**2.88**	**3.1**	**3.22**	**3.37**	**3.78**	**4**	**4.2**	**4.62**	**4.82**
Differential Output Swing (mV)	**964**	**986.4**	**1195**	**1099**	**997.8**	**893.4**	**799**	**769.2**	**884.2**	**712**
Total Power	**57 mA @ 1.8V**									
Process	**TSMC 0.18-µm CMOS**									
Chip Area	**2.5×1.4 mm^2**									

Table 3.4 Performance comparison of UWB frequency synthesizers

	This work	D. Leenaerts [14]	Jri Lee [15]
Frequency scheme	Dual conversion	Direct conversion	Direct conversion
Number of Bands	9 bands	3 bands	7 bands
LO frequency	6.336 ~10.56 GHz 2.904 GHz (IQ)	3.432 ~ 4.488 GHz	3.432 ~ 7.92 GHz
Switching time	< 1ns	<1ns	1ns
Sideband suppression	-43.1 @ 6.336 GHz	< -35 dBc	-37 dBc
Phase noise	< -126.7 dBc/Hz @ 10MHz	< -100 dBc/Hz @ 1 MHz	-110 dBc/Hz @ 1MHz (VCO)
Output swing	> 400 mVp-p Single-ended		
Supply voltage	1.8 V	2.7 V	2.2 V
Power consumption	57 mA	27.2 mA	48 mW
Technology	0.18-µm CMOS	0.25-µm SiGe BiCMOS	0.18-µm CMOS

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Chapter 4 HIGH FREQUENCY DIVIDERS

4.1 Introduction

High-frequency dividers play a crucial role in various broadband and wireless applications. On the one hand, high-speed frequency dividers are widely required to divide down high-frequency output signals from VCOs in phase-locked loops (PLLs) or synthesizers. On the other hand, divide-by-2 dividers are also commonly employed to achieve desired quadrature LO signals from a VCO operating at twice the frequency. Unlike QVCO solutions, dividers do not suffer from severe tradeoff between spectral purity and phase accuracy. The output phase noise of the divider is mainly determined by the input signal while the quadrature accuracy can be optimized by the divider itself.

Specifically, high-frequency dividers can be realized using common-mode logic (CML), using a Miller divider, or through the injection locking of oscillators. Miller dividers have been realized up to very high frequency with wide input bandwidth, unfortunately with a high power consumption [1]. Injection-locked (IL) dividers consume generally less power than Miller dividers due to the tuned nature of the circuit. However, one disadvantage of IL-dividers is the limited input locking range. On the other hand, injection-locked (IL) dividers [2] or regenerative (Miller) dividers [3], working as quadrature signals generator, have recently become quite attractive.

In this chapter, various types of injection-locked dividers with different input configurations as well as regenerative dividers will be presented. A double-balanced

quadrature-input quadrature-output regenerative (QIQO) divider is then proposed, which provides a mechanism to achieve an output IQ phase sequence that is inherently tracked with the input IQ phase sequence. Finally, two ultra-low-voltage (ULV) dividers with transformer-feedback or transformer-coupling are proposed and analyzed, which can operate at low-supply that is comparable to the device threshold voltage. In essence, a dual-loop feedback model is proposed and used to analyze all the dividers. The analyses of the output IQ phase sequence and the input frequency range of the dividers are emphasized.

4.2 Injection-Locked Dividers

It is well-known that, high-frequency VCOs can be modeled as closed-loop systems containing LC-tanks and feedback loops, as shown in Fig. 4.1.

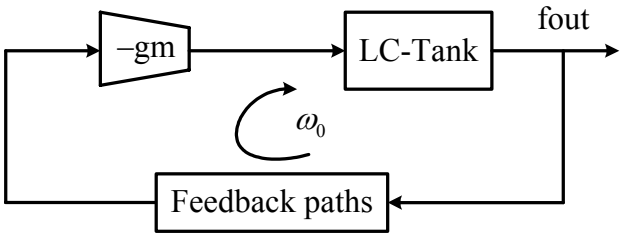


Fig. 4.1 Generic feedback model of VCOs

The self-oscillation frequency ω_0 of the VCO is then determined by the feedback system itself when satisfying the following conditions:

(1) The closed-loop gain at ω_0 must be equal to unity, or the open-loop gain at ω_0 is larger than one

(2) The total phase shift around the loop must be equal to zero

(3) With satisfied conditions (1) and (2), the close-loop system can have the

maximum output amplitude

In contrast, injection-locked (IL) dividers are constructed by self-oscillation loop (SOL) and additional frequency control loop (FCL) settled by external input signals. The divider function is realized by forcing the SOL to oscillate at a certain frequency that is fixed by the input frequency and its additional FCL. More specifically, it is accomplished by injecting both output currents from SOL and FCL into the LC-tank in the loop. Therefore, IL-dividers are also often referred as injection-locking oscillators. When there are no signals presented at the input side, IL-dividers, in fact, function as self-oscillators. On the other hand, the input frequency and the output frequency of an IL-divider are not equal. As a consequence, mixing operation in the FCL is necessary. In general, there are two methods to implement the required FCL. Fig. 4.2 illustrates one of the possible architectures for IL-dividers, in which the FCL is shared with SOL. Furthermore, both operations can be achieved by the same active devices, such as the most frequently used topology shown in [2].

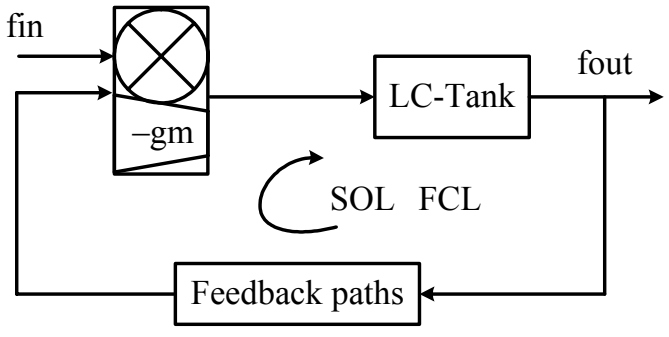


Fig. 4.2 System block diagram of IL-dividers (Case 1)

Another implementation of the IL-divider is to include two independent SOL and FCL. As shown in Fig. 4.3, extra mixer and feedback paths are included in the

FCL. The mixer, however, could be any types of passive or active mixers including both single-balanced and double-balanced configurations. For instance, the direct injection-locked oscillator proposed in [4] belongs to this case. Of course, an IL-divider can contain both above mentioned cases as well.

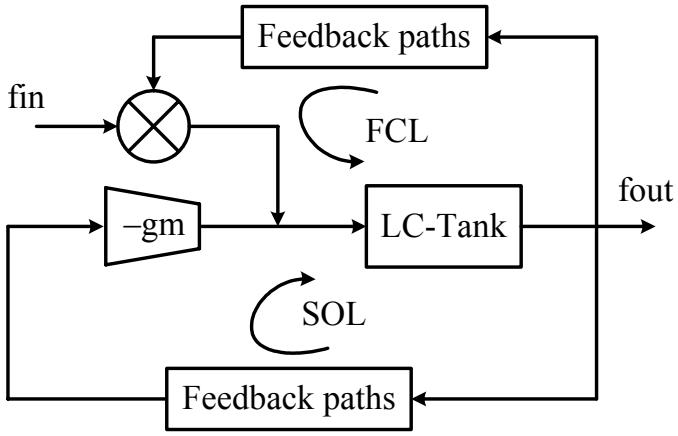


Fig. 4.3 System block diagram of IL-dividers (Case 2)

In the following section, more circuit-level implementations of IL-dividers will be addressed.

4.2.1 Conventional Injection-locked Divider Architecture

Fig. 4.4 shows a conventional VCO based divide-by-2 IL-divider topology, wherein the input signal is applied at DC biasing transistor M3 in the VCO. On the one hand, the transistors M1~M3 can be treated as a single-balanced mixer. On the other hand, they are parts of the VCO components as well. Consequently, the conventional IL-divider can be modeled as a single-loop feedback system, as shown in Fig. 4.5. The mixer's input current is the combination results of the DC biasing current and the double frequency injected signal, which are relevant to the components in the SOL and the FCL respectively.

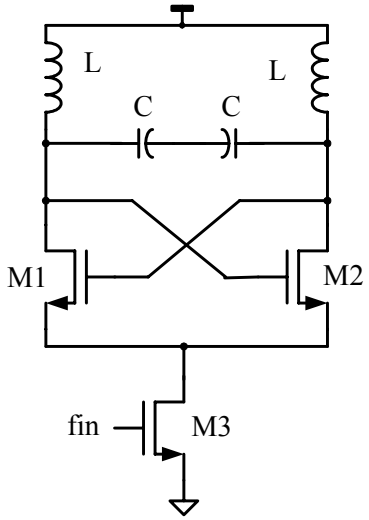


Fig. 4.4 Schematic of the conventional IL-divider

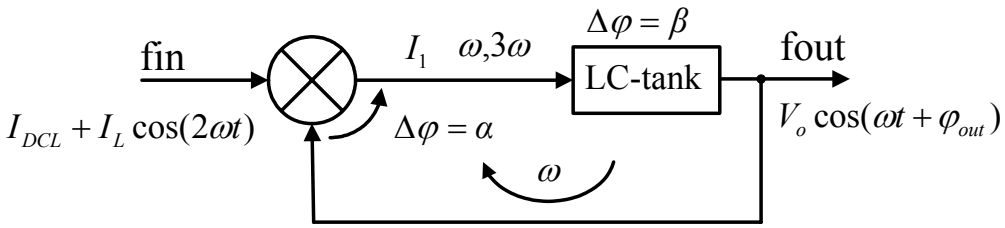


Fig. 4.5 Feedback loop model of the conventional IL-divider

In order for the divider to operate properly, the following conditions are necessary [1]: 1) The total phase shift around the loop at the operation frequency ω must be zero; 2) The loop gain at ω must be at least unity; and 3) There is enough suppression of the third-harmonic. Assuming that the phase shift introduced by the LC-tank is β, the mixer is required to introduce another phase shift α so that

$$\alpha + \beta = 0 \tag{4.1}$$

To gain intuitive understanding of how the loop can sustain stable oscillation when locked by the input injected signal, the first necessary condition of zero-phase shift in the loop is the focus in our analyses. Assume that the divider output signal is expressed by $V_o \cos(\omega t + \varphi_{out})$ with an output phase φ_{out}, the mixer's output current is given by

$$
\begin{aligned}
I_1 &= \left[I_{DCL} + I_L \cos(2\omega t)\right] \times V_o \cos(\omega t + \varphi_{out}) \\
&= I_{DCL} V_o \cos(\omega t + \varphi_{out}) + 1/2\, I_L V_o \left[\cos(3\omega t + \varphi_{out}) + \cos(\omega t - \varphi_{out})\right]
\end{aligned} \tag{4.2}
$$

As observed from Eq. (4.2), the output current comprises two components: the DC current multiplying element with no phase shift, and the injected signal mixing term with an inverted phase. In general, the AC current is less than two times of the DC current, as expressed by $I_L < 2I_{DCL}$. The maximum phase shift α_{max}, the mixer can provide, is actually limited by the DC mixing term. To obtain more insight into the phase shift around the loop, Fig. 4.6 plots the phase diagram of the mixer's output current without taking the 3rd-order term into account.

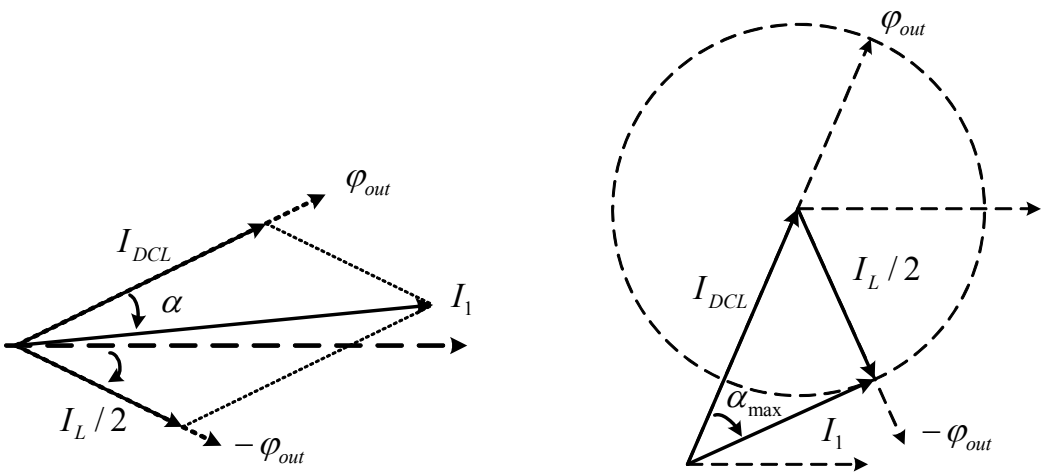


Fig. 4.6 Phase diagram of the mixer's output current

Obviously, the maximum phase shift α_{max} can be derived from the phase diagram shown in Fig. 4.6. That is

$$
\left|\alpha_{\max}\right| = \arcsin\left(\frac{I_L}{2I_{DCL}}\right) \tag{4.3}
$$

By defining the input AC to DC current injection ratio of $\eta = \frac{I_L}{I_{DCL}}$, Eq. (4.3) is rearranged as

$$|\alpha_{\max}| = \arcsin\left(\frac{\eta}{2}\right) \tag{4.4}$$

Equation (4.4) implies that a larger injection ratio leads to a wider achievable phase shift by the mixer in the loop.

In addition, as illustrated in Fig. 4.4 and Fig. 4.5, the mixer's output current is injected into the LC-tank, and hence induces another phase shift of β. By defining the finite quality factor Q of the LC-tank to be the peak frequency over -3dB bandwidth, the impedance of the LC-tank can be expressed by

$$Z(\omega) = \frac{Z_p}{1 + j2Q(\omega - \omega_p)/\omega_p} \tag{4.5}$$

where Z_p and ω_p denote the peak impedance and peak frequency of the LC-tank, respectively. As a result, the phase shift induced by the LC-tank is derived as

$$\beta = -\arctan(2Q\frac{\omega - \omega_p}{\omega_p}) \tag{4.6}$$

From Eqs. (4.1), (4.4) and (4.6), the maximum potential operation range of the IL-divider is hence derived as

$$\frac{\Delta\omega}{\omega_p} = \frac{1}{Q\sqrt{\frac{4}{\eta^2} - 1}} \approx \frac{\eta}{2Q} \tag{4.7}$$

which is limited by the first necessary condition mentioned previously for a divider to operate successfully. From Eq. (4.7), we can conclude that the maximum potential input locking range of the IL-divider is increased by increasing the injection ratio η, or reducing the tank quality factor Q to tradeoff the larger power consumption.

In summary then, the IL-divider can benefit from small power consumption but

need to sacrifice the input locking range. Furthermore, if aiming at the fully-integration of a differential VCO and an IL-divider, the single-ended input in the conventional IL-divider is very disadvantageous. On the other hand, when quadrature output signals are needed in the design, two identical IL-dividers driven by differential signals can be implemented. As such, the disadvantage of the single-ended input for a single IL-divider is compensated and eliminated. Fig. 4.7 shows the circuit implementation of two IL-dividers for quadrature outputs generation, wherein the input transistors M5 and M6 are driven by anti-phase signals. To gain better understanding on how the anti-phase inputs can result in the 90^o phase difference at two dividers outputs, the feedback model shown in Fig. 4.5 is adopted for our analysis.

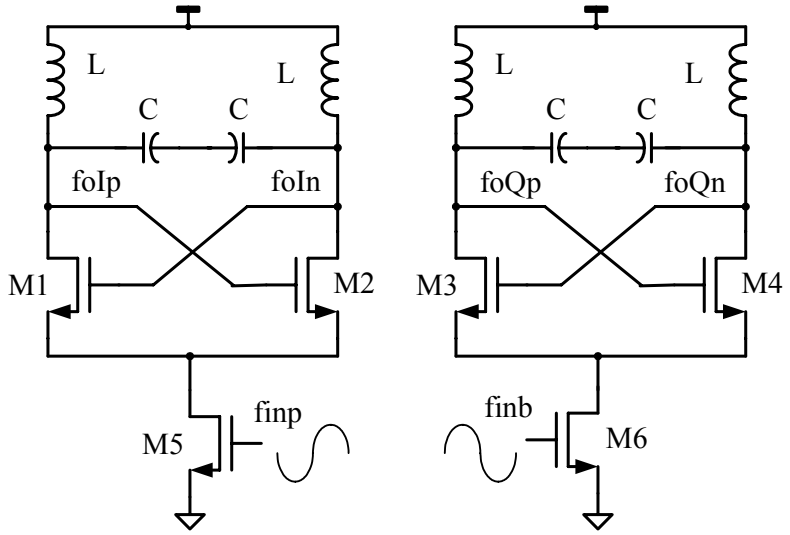


Fig. 4.7 Schematic of two IL-dividers with quadrature outputs

By assuming an input initial phase of φ_{in}, Eq. (4.2) is hence rewritten as

$$\begin{aligned} I_1^{"} &= \left[I_{DCL} + I_L \cos(2\omega t + \omega_{in})\right] \times V_o \cos(\omega t + \varphi_{out}^{"}) \\ &= I_{DCL} V_o \cos(\omega t + \varphi_{out}^{"}) + 1/2\, I_L V_o \left[\cos(3\omega t + \omega_{in} + \varphi_{out}^{"}) + \cos(\omega t + \omega_{in} - \varphi_{out}^{"})\right] \end{aligned} \quad (4.8)$$

where $\varphi_{out}^{"}$ presents the divider output phase which is relevant to the input initial

phase of φ_{in}.

From Eq. (4.1), under locked situation, the phase shift α must keep in constant for an arbitrary initial phase of the input signal. Consequently, the phase shift α_2, as shown in Fig. 4.8, is a fixed value as well. Therefore, from Eqs. (4.2) and (4.8), we have

$$\alpha_2 = \omega_{in} - 2\varphi''_{out} = -2\varphi_{out} \tag{4.9}$$

Rearranging (4.9) into

$$\varphi''_{out} = \varphi_{out} + \frac{\omega_{in}}{2} \tag{4.10}$$

As explained by Eq. (4.10), an 180^o phase change of the input signal will lead to an output phase deviation of 90^o. In other words, the quadrature signals can be obtained from two identical IL-dividers driven by two anti-phase input signals. Nevertheless, there is no deterministic quadrature phase sequence. In addition, equation (4.10) also implies that the output IQ phase accuracy of the IL-divider is directly affected by the differential phase mismatch of the input signals, as expressed by

$$\lambda_{in} = \theta_{in}/2 \tag{4.11}$$

Here λ_{in} is the quadrature-output phase mismatch due to the differential-input phase mismatch, and θ_{in} is the differential phase mismatch of the anti-phase input signals.

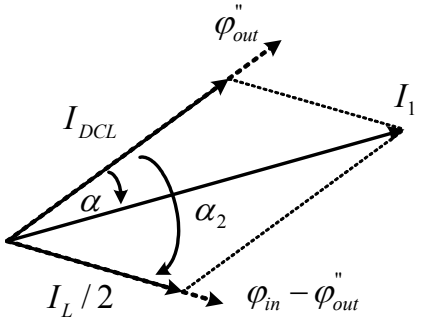


Fig. 4.8 Phasor diagram with an input initial phase of φ_{in}

Another dominated contribution to the output phase error comes from the mismatches in their LC-tanks, which could be caused either by the capacitive mismatch or by the inductive mismatch. To gain insight into the sensitivity, we can assume that a phase shift mismatch ($\Delta\beta$) of θ_{lc} exists between two LC-tanks. According to Eq. (4.1), the phase shift mismatch $\Delta\beta$ needs to be compensated by the phase shift α provided by the mixer, and having a relation of $\Delta\alpha=\Delta\beta=\theta_{lc}$.

From Fig. 4.8 we can calculate the output current I_1 as

$$I_1^{\,2} = I_{DCL}^{\,2} + I_L^{\,2}/4 + I_{DCL} I_L \cos(2\varphi_{out}^{"} - \varphi_{in}) \tag{4.12}$$

Thus, the phase shift α is given by

$$\cos(\alpha) = \frac{\left[2I_{DCL} + I_L \cos(2\varphi_{out}^{"} - \varphi_{in})\right]}{2\sqrt{I_{DCL}^{\,2} + I_L^{\,2}/4 + I_{DCL} I_L \cos(2\varphi_{out}^{"} - \varphi_{in})}} \tag{4.13}$$

Likewise, we have

$$\cos(\alpha + \Delta\alpha) = \frac{\left[2 + \eta\cos\left(2(\varphi_{out}^{"} + \lambda_{lc}) - \varphi_{in}\right)\right]}{2\sqrt{1 + \eta^2/4 + \eta\cos\left(2(\varphi_{out}^{"} + \lambda_{lc}) - \varphi_{in}\right)}} \tag{4.14}$$

And λ_{lc} is the output phase deviation $\Delta\varphi_{out}$. Eq. (4.14) can be further approximated to

$$\cos(\alpha + \Delta\alpha) \approx \sqrt{1 + \frac{\eta}{2}\cos\left(2(\varphi_{out}^{"} + \lambda_{lc}) - \varphi_{in}\right)} \tag{4.15}$$

Therefore, we can find that the quadrature-output phase mismatch of two

IL-dividers is inversely proportional to the injection ration η. The above analyses for the conventional IL-divider show that increasing the injection ration η not only enlarges the input locking range, but also simultaneously enhances the quadrature-output phase accuracy.

4.2.2 Injection-locked Divider With Quadrature-coupled Pairs

From the analyses given in the previous section, two conventional identical IL-dividers driven by two anti-phase input signals can be implemented to realize divide-by-2 function for fully-differential input signals, or to achieve required quadrature outputs. All in all, the conventional IL-divider provides the lowest power consumption but suffering from the limited locking range and the random output IQ phase sequence. To deal with the potential problem due to the undetermined phase sequence, additional quadrature-coupled (QC) devices can be added into the two identical dividers. As shown in Fig. 4.9, the QCIL-divider contains two simplest IL-dividers and quadrature-coupled loops in between.

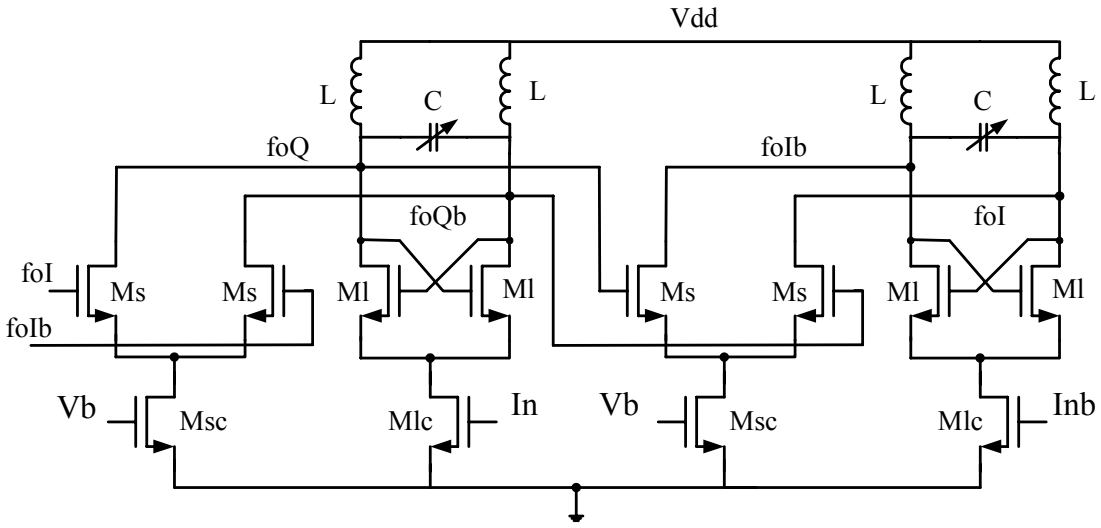


Fig. 4.9 Schematic of the IL-divider with quadrature-coupled pairs

Similar to the differential-coupled transistor Ml, the quadrature-coupled pair Ms

also can be modeled as a mixer but only mixing with DC current. Fig. 4.10 illustrates the full feedback model of the QCIL-divider, in which the output signals are represented by $V_{oQ}\cos(\omega t+\varphi_{outQ})$ and $V_{oI}\cos(\omega t+\varphi_{outI})$ respectively. The DC current terms for quadrature-coupled part and differential-coupled part are denoted by I_{DCS} and I_{DCL} respectively. The DC current ratio as well as the transistor size ratio of Ms to Ml is defined as

$$I_{DCS}/I_{DCL}=K_{SL} \tag{4.16}$$

Without considering the mismatches between I and Q parts, we can assume that $\beta=\beta_Q=\beta_I$, and $V_o=V_{oQ}=V_{oI}$.

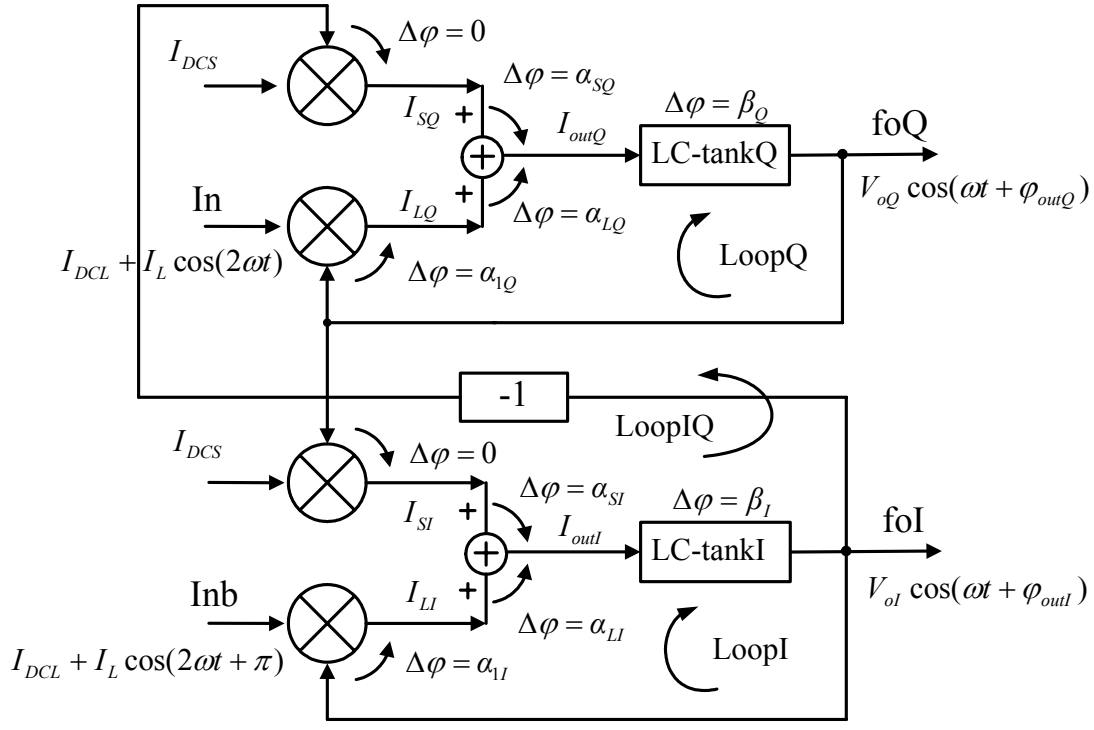


Fig. 4.10 Full feedback model of the QCIL-divider

In order for the divider to operate properly, the total phase shift around all the loops must be zero. As shown in Fig. 4.10, the QCIL-divider is represented by 3 different feedback loops in the model: Loop Q in the Q-output part, Loop I in the

I-output part, and Loop IQ crossing both Q- and I-part. As a consequence, we have

$$\alpha_{1Q} + \alpha_{LQ} + \beta = 0 \tag{4.17}$$

$$\alpha_{1I} + \alpha_{LI} + \beta = 0 \tag{4.18}$$

$$\alpha_{SQ} + \beta + \alpha_{SI} + \beta + \pi = 0 \tag{4.19}$$

On the other hand, we can observe the following relations:

$$\alpha_{1Q} + \alpha_{LQ} = \varphi_{IoutQ} - \varphi_{outQ}, \quad \alpha_{1I} + \alpha_{LI} = \varphi_{IoutI} - \varphi_{outI},$$

$$\alpha_{SQ} = \varphi_{IoutQ} - \varphi_{outI} - \pi, \text{ and } \quad \alpha_{SI} = \varphi_{IoutI} - \varphi_{outQ}$$

Consequently, we obtain

$$\alpha_{SQ} + \alpha_{SI} = \alpha_{1Q} + \alpha_{LQ} + \alpha_{1I} + \alpha_{LI} - \pi \tag{4.20}$$

From Eq. (4.20), we can draw the conclusion that as long as Eqs. (4.17) and (4.18) are satisfied, Eq. (4.19) is fulfilled intrinsically. In other words, only the zero-phase-shift requirements around the Loop Q and Loop I need to be taken into account.

The mixer's output current I_{LQ} and the summed current I_{outQ} in Loop Q are expressed by

$$\begin{aligned} I_{LQ} &= \left[I_{DCL} + I_L \cos(2\omega t)\right] \times V_o \cos(\omega t + \varphi_{outQ}) \\ &= I_{DCL} V_o \cos(\omega t + \varphi_{outQ}) + 1/2\, I_L V_o \left[\cos(3\omega t + \varphi_{outQ}) + \cos(\omega t - \varphi_{outQ})\right] \end{aligned} \tag{4.21}$$

$$I_{outQ} = I_{LQ} + I_{SQ} = I_{LQ} + I_{DCS} V_o \cos(\omega t + \varphi_{outI} + \pi) \tag{4.22}$$

Likewise, the mixer's output current I_{LI} and the summed current I_{outI} in Loop I are given by

$$\begin{aligned} I_{LI} &= \left[I_{DCL} + I_L \cos(2\omega t + \pi)\right] \times V_o \cos(\omega t + \varphi_{outI}) \\ &= I_{DCL} V_o \cos(\omega t + \varphi_{outI}) + 1/2\, I_L V_o \left[\cos(3\omega t + \varphi_{outI} + \pi) + \cos(\omega t - \varphi_{outI} + \pi)\right] \end{aligned} \tag{4.23}$$

$$I_{outI} = I_{LI} + I_{SI} = I_{LI} + I_{DCS} V_o \cos(\omega t + \varphi_{outQ}) \tag{4.24}$$

To gain better understanding of the phase change around the loops, Fig. 4.11 plots the phasor diagram both for the currents in Loop Q and Loop I.

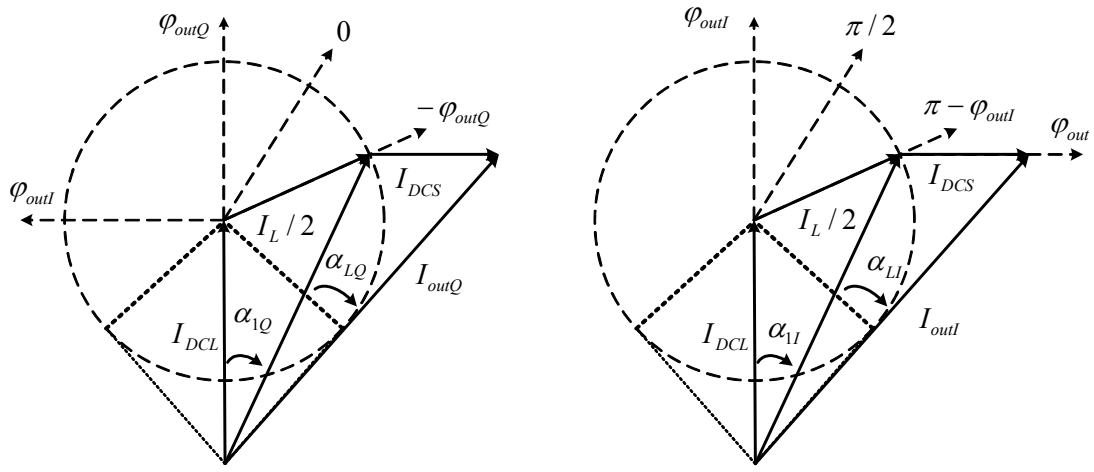


Fig. 4.11 Phasor diagram of (a) the currents in Loop Q, and (b) the currents in Loop I

If all the components in Loop Q and Loop I are perfectly matched, the output currents I_{outQ} and I_{outI} as well as the total phase shift in both loops are equal. As such, the Q-output phase is deviated from the I-output phase by 90^o, as explained in Fig. 4.11. Nevertheless, taking the fact that the anti-phase input signal could be shown as $I_L \cos(2\omega t \pm \pi)$ in Eq. (4.23), the output IQ phase sequence could appear in Q leading I or Q lagging I, which is actually set by the phase shift β from the LC-tank. To explore the connections between the output phase sequence and the phase shift from the LC-tank, Fig. 4.12 illustrates all the possible phasor for the output current I_{outQ}. Here, a perfect quadrature output phase is first assumed.

When $\beta > 0$, the loop is needed to provide negative phase shift to meet the requirement shown in Eq. (4.17). The Q-output phase hence lags I-output phase by 90^o. Similarly, when $\beta < 0$, the divider Q-output signal leads the I-output signal by 90^o. In addition, from Eq. (4.6), the LC-tank's phase shift $\beta < 0$ when the operation

frequency $\omega > \omega_p$, and $\beta > 0$ when $\omega < \omega_p$. It follows that when the divider output frequency ω_{out} is lower than peak frequency ω_p, the Q-output signal lags the I-output signal by 90^o. Similarly, when ω_{out} is higher than ω_p, the Q-output signal leads the I-output signal by 90^o.

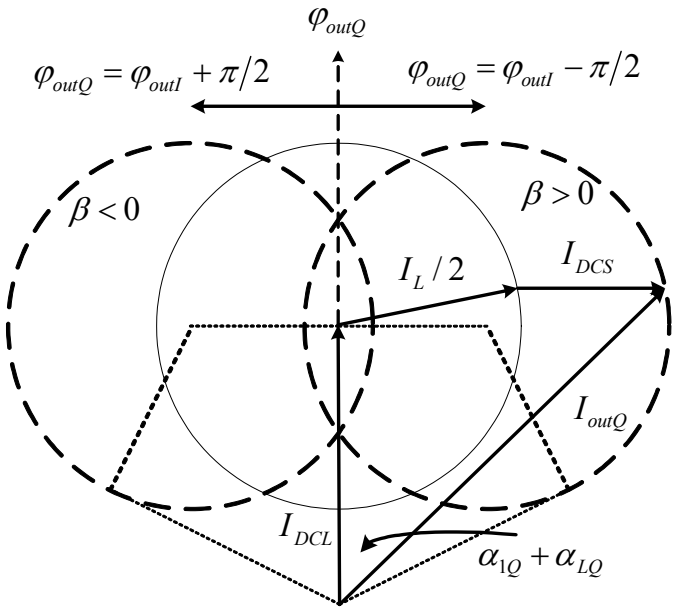


Fig. 4.12 The potential phasor of the output current I_{outQ}

Moreover, from Fig. 4.12, we also can write the maximum potential phase shift as below

$$|\beta|_{\max} = |\alpha_{1Q} + \alpha_{LQ}|_{\max} = \arctan\left(\frac{I_{DCS}}{I_{DCL}}\right) + \arcsin\left(\frac{I_L}{2\sqrt{I_{DCS}^2 + I_{DCL}^2}}\right) \tag{4.25}$$

Defining the injection ratio of $\eta = \frac{I_L}{I_{DCL}}$, and substituting (4.16) to (4.25), we have

$$|\beta|_{\max} = \arctan(K_{SL}) + \arcsin\left(\frac{\eta}{2\sqrt{1 + K_{SL}^2}}\right) \tag{4.26}$$

By comparing Eqs. (4.4) and (4.26), it is concluded that the QCIL-divider has wider potential locking rang than the simplest one analyzed in section 4.2.1.

On the other hand, if $I_{DCS} < I_L/2$, the minimum able-compensated phase shift

β is zero. Whereas, if $I_{DCS} > I_L/2$, the minimum β becomes

$$|\beta|_{\min} = \arctan(K_{SL}) - \arcsin\left(\frac{\eta}{2\sqrt{1+K_{SL}^2}}\right) \tag{4.27}$$

That means, for the scenario of $I_{DCS} > I_L/2$, there is a gap near the center frequency of the LC-tank in which the QCIL-divider can not perform divide-by-2 function. Still, the gap can be narrowed or covered by increasing the injected AC current of the divider. Furthermore, Fig. 4.12 implies extra information as well: the QCIL-divider may fail to provide good quadrature phase at or near the center frequency of the LC-tank, since the divider does not contain clear information about the quadrature phase sequence at that region.

4.2.3 Injection-locked Divider With Differential Inputs

In the previous QCIL-divider, the input AC signal is only applied at the differential-coupled part M_{lc}. However, an alternative way to realize the frequency control loop is to inject the AC input both to the quadrature-coupled (QC) part and the differential-coupled (DC) part simultaneously. As shown in Fig. 4.13, both transistors M_{sc} and M_{lc} in QC-pairs and DC-pairs are driven by differential input signals.

With the same analysis performed for the QCIL-divider, given the condition of perfectly matched devices at I- and Q-parts, we can approve that the differential-input IL-divider (DIIL-divider) can deliver quadrature phase at outputs. The Q-output part of the DIIL-divider is represented by the dual-loop feedback model shown in Fig. 4.14, wherein the Q-output could be either lead or lag the I-output by 90^o.

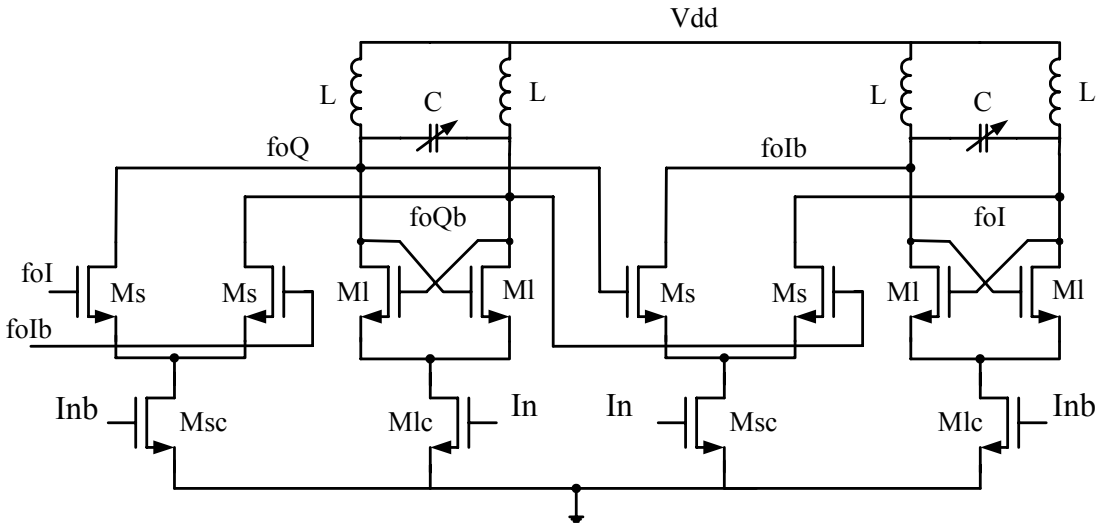


Fig. 4.13 Schematic of the IL-divider with QC-part and DC-part both having differential inputs

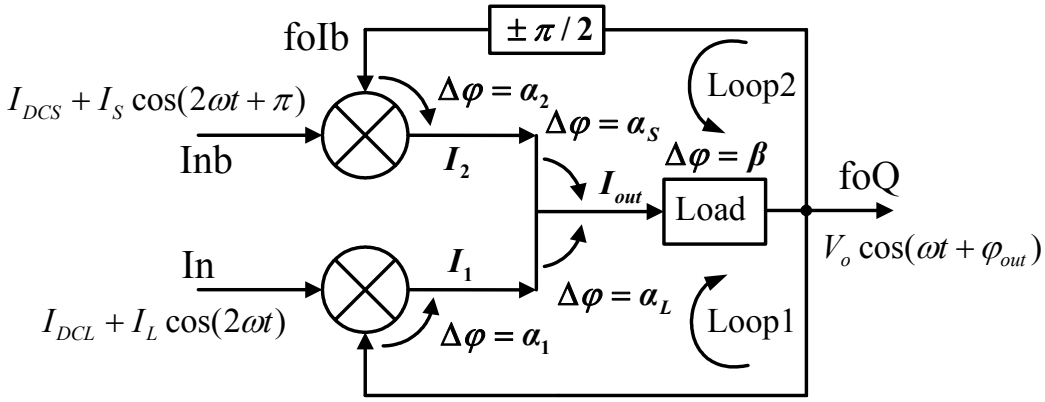


Fig. 4.14 Dual-loop feedback model of the Q-output part of the DIIL-divider

The relevant output current in the loops are hence derived as below:

$$I_1 = I_{DCL}V_o\cos(\omega t + \varphi_{out}) + 1/2\, I_L V_o\left[\cos(3\omega t + \varphi_{out}) + \cos(\omega t - \varphi_{out})\right] \tag{4.28}$$

$$I_2 = I_{DCS}V_o\cos(\omega t + \varphi_{out} + \pi/2) + 1/2\, I_S V_o\begin{bmatrix}\cos(3\omega t + \varphi_{out} + 3\pi/2)\\ +\cos(\omega t - \varphi_{out} + \pi/2)\end{bmatrix} \tag{4.29}$$

with +90^o phase shift in Loop 2, or

$$I_2 = I_{DCS}V_o\cos(\omega t + \varphi_{out} - \pi/2) + 1/2\, I_S V_o\begin{bmatrix}\cos(3\omega t + \varphi_{out} + \pi/2)\\ +\cos(\omega t - \varphi_{out} - \pi/2)\end{bmatrix} \tag{4.30}$$

with -90^o phase shift in Loop 2.

Note that, the phasor of the mixer's output current I_1 has 90^o phase deviation from current I_2. In addition, both input currents in Loop 1 and Loop 2 have the same AC to DC ratio, which results in the I_2 to I_1 ratio of

$$\frac{I_2}{I_1} = \frac{I_{DCS}}{I_{DCL}} = K_{SL} \tag{4.31}$$

Fig. 4.15 plots the phasor diagram of the output currents for better understanding.

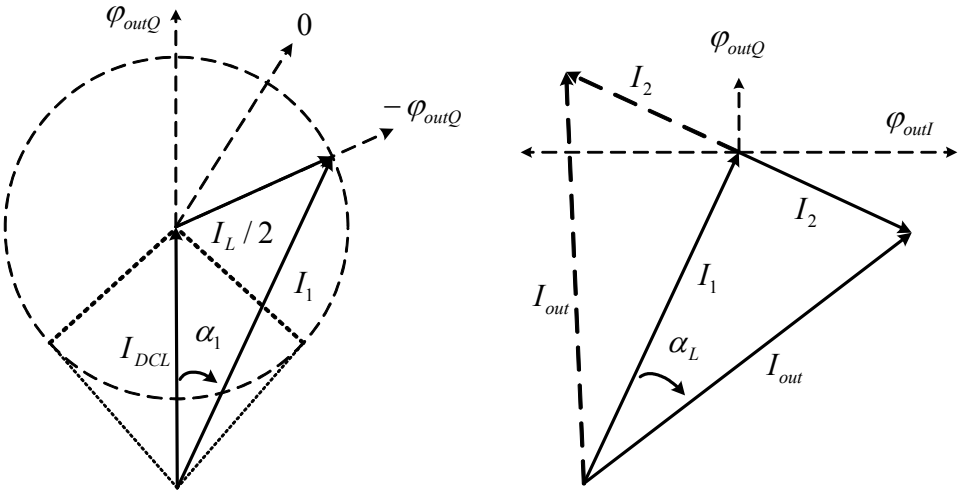


Fig. 4.15 Phasor diagram of the output currents in Loop 1

In Loop 1, assuming that the phase shift introduced by the LC tank is β, and the phase shift contributed by addition of the two mixers output current is α_L, then the mixer in Loop 1 is required to introduce another phase shift α_1 so that $\alpha_1 + \alpha_L + \beta = 0$. From Eq. (4.31) as well as from Fig. 4.15, the phase shift formed by the current adding of I_1 and I_2 is computed to be

$$\alpha_L = \pm \arctan(K_{SL}) \tag{4.32}$$

And the output current becomes

$$I_{out} = \sqrt{I_1^2 + I_2^2} = I_1\sqrt{1 + K_{SL}^2} \tag{4.33}$$

On the other hand, as shown in Fig. 4.15, the mixer output current I_1 is inversely

proportional to the phase shift $|\alpha_1|$. The final output current I_{out} which is injected into the LC-tank, is hence inversely proportional to the phase shift $|\alpha_1|$ as well. Remembering that the oscillation in a closed-loop system appears at the situation where the loop can have maximum output amplitude, while satisfying the zero phase shift and gain requirements. In other words, the DIIL-divider will operate at the minimum phase shift of $|\alpha_1|$. Therefore, the mixer's phase shift in Loop 1 becomes

$$\alpha_1 = -\min(|\alpha_L + \beta|) \tag{4.34}$$

When $\beta > 0$, $\alpha_L = -\arctan(K_{SL})$, and the divider Q-output signal lags I signal by 90^o. Similarly, when $\beta < 0$, $\alpha_L = +\arctan(K_{SL})$, and the divider Q-output signal leads the I signal by 90^o. Likewise, we obtain the same conclusion as the one in the QCIL-divider: when the divider output frequency ω_{out} is lower than peak frequency ω_p, the Q-output signal lags the I-output signal by 90^o; when ω_{out} is higher than ω_p, the Q-output signal leads the I-output signal by 90^o. Still, just as the same case in the QCIL-divider, the DIIL-divider may fail to provide good quadrature phase at or near the center frequency of the LC-tank.

Furthermore, the maximum phase shift from LC-tank, which is able-compensated by the loop, is given by

$$|\beta|_{\max} = \arctan(K_{SL}) + \arcsin\left(\frac{\eta}{2}\right) \tag{4.35}$$

It is actually larger than the one obtained in the QCIL-divider. Similarly, the minimum phase shift provided by the mixer and current adding is zero when $\arctan(K_{SL}) < \arcsin\left(\frac{\eta}{2}\right)$. Alternatively, when $\arctan(K_{SL}) > \arcsin\left(\frac{\eta}{2}\right)$, we

have

$$|\beta|_{\min} = \arctan(K_{SL}) - \arcsin\left(\frac{\eta}{2}\right) \tag{4.36}$$

As a result, when the injection ratio η is small, the DIIL-divider may fail to function at the nearby region of the center frequency of the LC-tank.

One design of the DIIL-divider has been implemented in the UWB frequency synthesizer proposed in Chapter 3. The DIIL-divider is employed to achieve the required 2nd IQ LO signals at 2.904 GHz. The transistor size ratio of the quadrature-coupled part to differential-coupled part (K_{SL}) is optimized to be 1/2. Fig. 4.16 shows the die photography of the DIIL-divider in the synthesizer, which is designed and fabricated in TSMC 0.18-μm CMOS process with 6 metal layers.

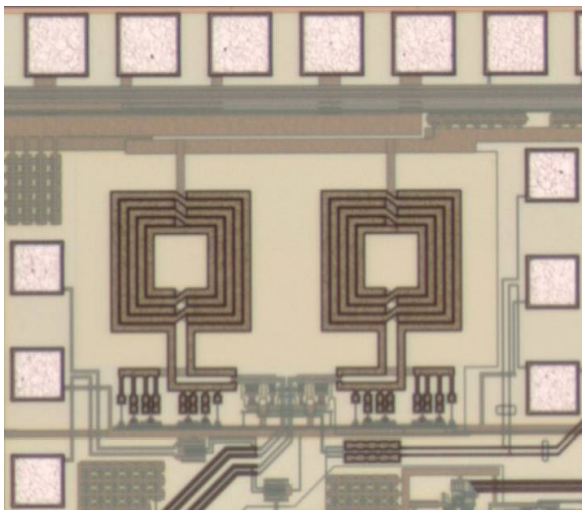


Fig. 4.16 Die photography of the DIIL-divider in the UWB synthesizer

The peak frequency of the LC-tank is located at around 3 GHz. Fig. 4.17 plots the measured output power versus the input frequency at various input power levels. As expected, when the input power as well as the injection ratio η of the divider is small, the DIIL-divider does not function at the peak frequency region of the

LC-tank. Thus, the input locking range is broken into two sections. While, as the input power increases continuously, the gap between two sections is getting smaller and smaller. Finally, two sections of the input locking range become merged.

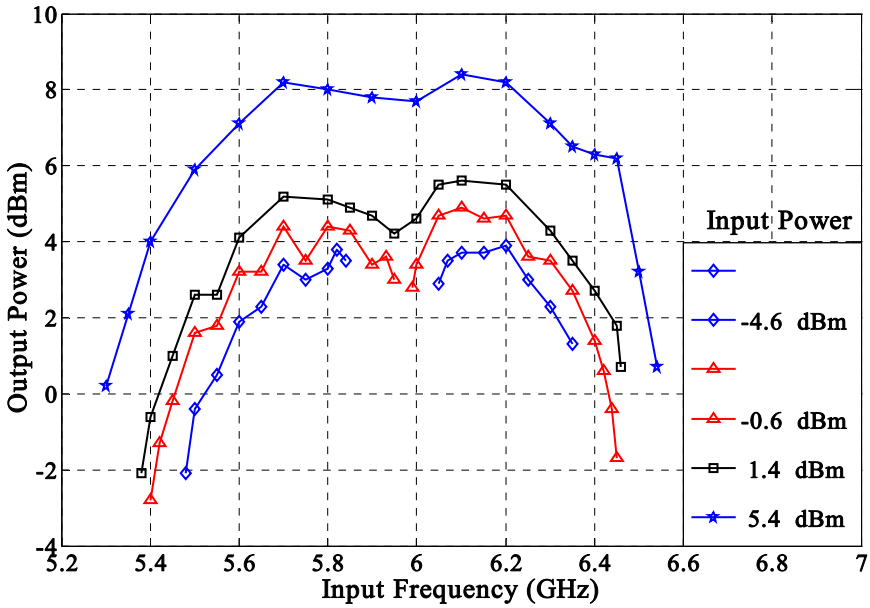
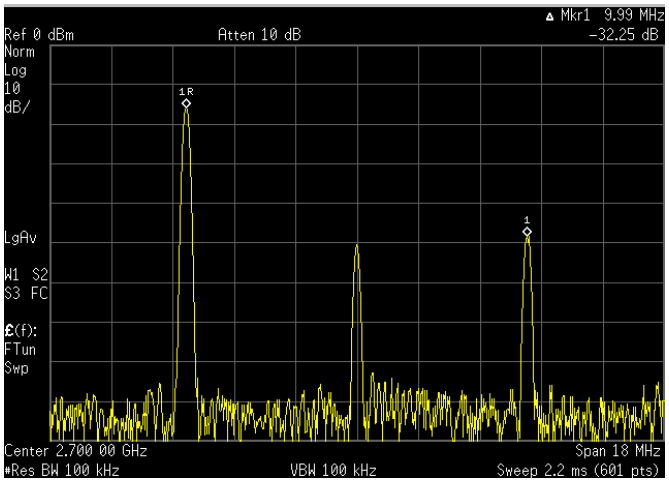
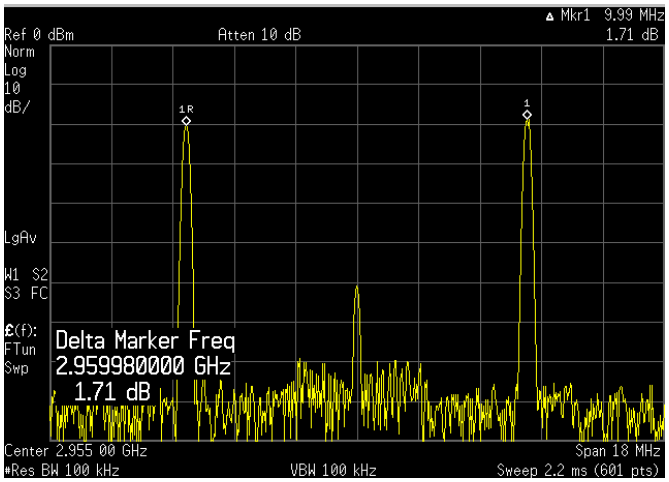


Fig. 4.17 Measured output power VS. input frequency at various input power levels

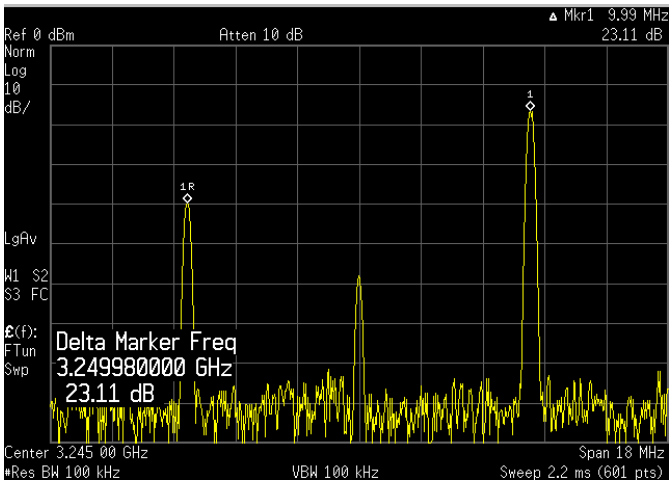
To verify the phase accuracy of the quadrature signals generated by the DIIL-divider, an on-chip SSB mixer is included to measure the sideband rejection. Agilent E4438C vector signal generator is used to generate the IQ baseband signals at 5 MHz. Fig. 4.18 shows the measured output sideband rejections at three different output frequencies. As shown in Fig. 4.18(b), the DIIL-divider actually can not deliver quadrature outputs at center frequency of the LC-tank. Moreover, the divider measures the reversed sideband output for the output frequencies which are below and above the center frequency of the LC-tank, which are shown in Fig. 4.18(a) and (c) respectively. Indeed, these results are consistent with the aforementioned analysis.



(a) Sideband rejection at 2.7 GHz output



(b) Sideband rejection at 2.955 GHz output



(c) Sideband rejection at 3.245 GHz output

Fig. 4.18 Measured output sideband rejections of the DIIL-divider at three different output frequencies

4.2.4 Injection-locked Divider With Quadrature Inputs

In contrast to the DIIL-divider driven by fully differential signals, the quadrature-coupled part of the divider can be driven by a quadrature-phase signal as well, which is shown in Fig. 4.19.

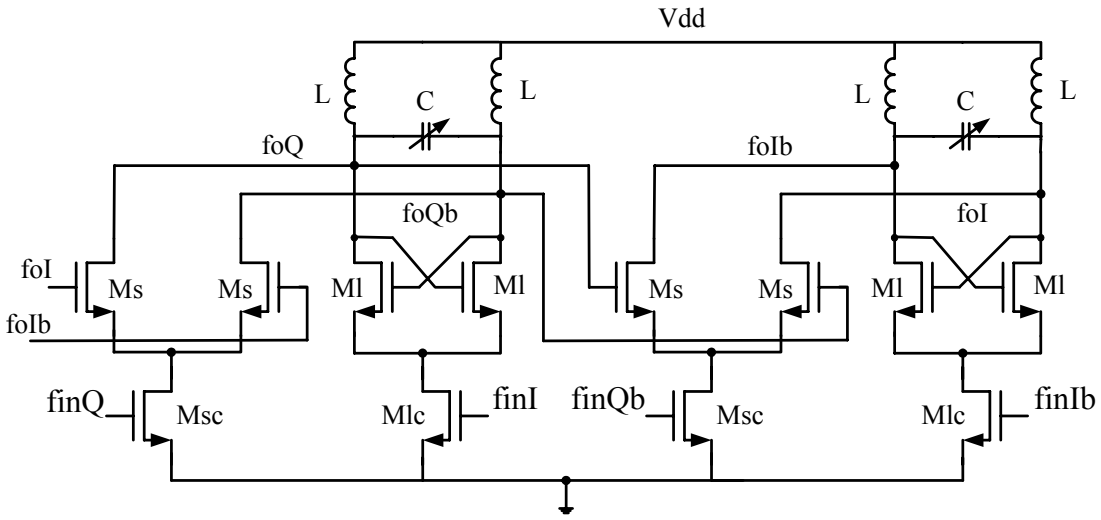


Fig. 4.19 Schematic of the IL-divider with quadrature input signals

Given the fact that the divider's IQ-output will appear in quadrature, Fig. 4.20 illustrates the dual-loop feedback model for the Q-output part of the quadrature-input IL-divider (QIIL-divider).

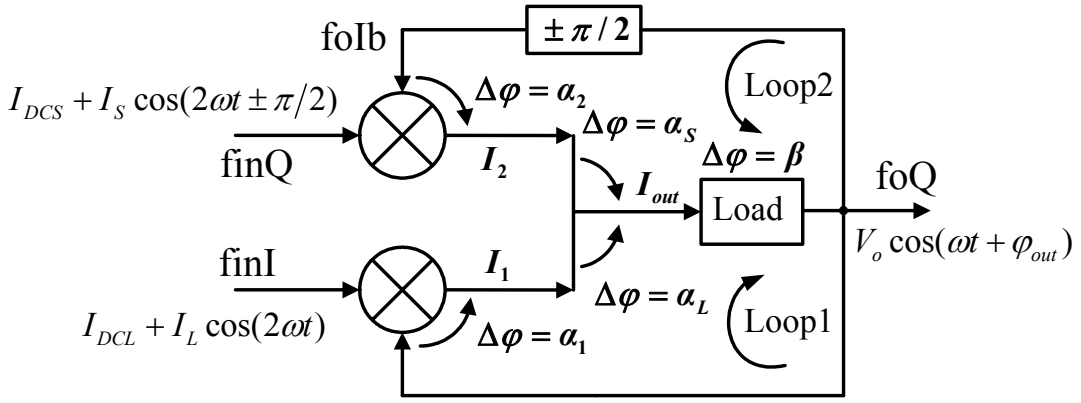


Fig. 4.20 Dual-loop feedback model for the Q-output part of the QIIL-divider

As known to all, quadrature input signals have two possible IQ phase sequences, which are finQ leads finI or finQ lags finI by 90°. Nevertheless, two opposite input

phase sequences will lead to two entirely different operation performances of the divider. The relevant output currents are shown as follows:

$$I_1 = I_{DCL}V_o\cos(\omega t+\varphi_{out})+1/2\,I_L V_o\left[\cos(3\omega t+\varphi_{out})+\cos(\omega t-\varphi_{out})\right] \quad (4.37)$$

$$I_2 = I_{DCS}V_o\cos(\omega t+\varphi_{out}+\pi/2)+1/2\,I_S V_o\left[\cos(3\omega t+\varphi_{out}+\pi)+\cos(\omega t-\varphi_{out})\right] \quad (4.38)$$

$$\text{or } I_2 = I_{DCS}V_o\cos(\omega t+\varphi_{out}-\pi/2)+1/2\,I_S V_o\left[\cos(3\omega t+\varphi_{out})+\cos(\omega t-\varphi_{out}+\pi)\right] \quad (4.39)$$

For the case of $finQ = I_{DCS}+I_S\cos(2\omega t+\pi/2)$;

And

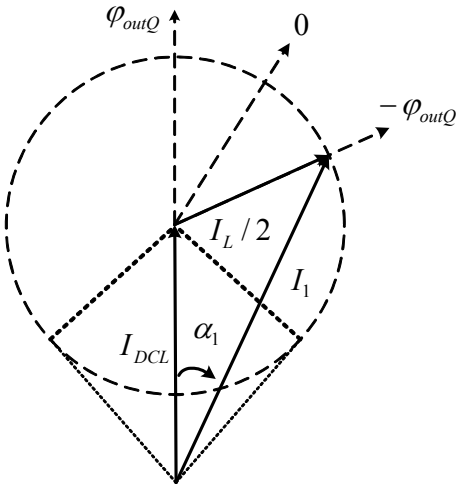
$$I_2 = I_{DCS}V_o\cos(\omega t+\varphi_{out}+\pi/2)+1/2\,I_S V_o\left[\cos(3\omega t+\varphi_{out})+\cos(\omega t-\varphi_{out}-\pi)\right] \quad (4.40)$$

$$\text{or } I_2 = I_{DCS}V_o\cos(\omega t+\varphi_{out}-\pi/2)+1/2\,I_S V_o\left[\cos(3\omega t+\varphi_{out}-\pi)+\cos(\omega t-\varphi_{out})\right] \quad (4.41)$$

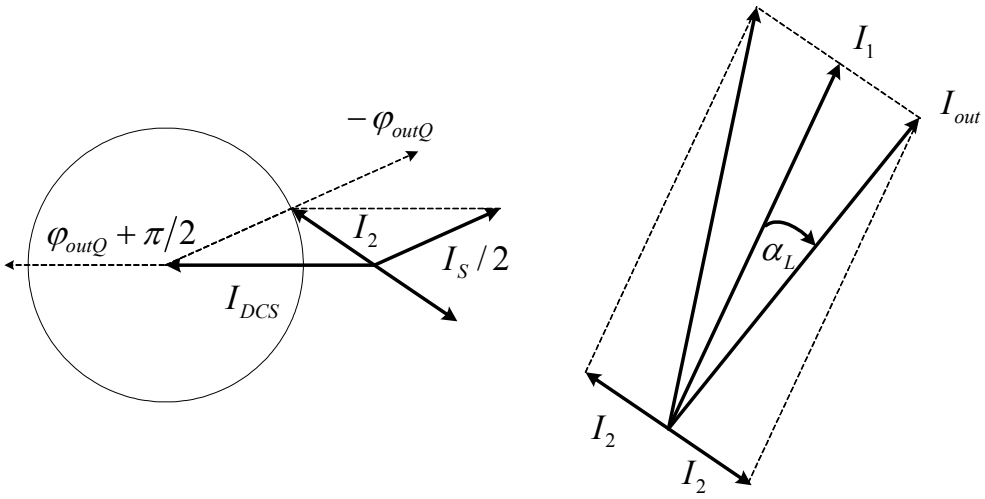
For the case of $finQ = I_{DCS}+I_S\cos(2\omega t-\pi/2)$;

Fig. 4.21 shows the phasor diagram for all the above output currents for more insight.

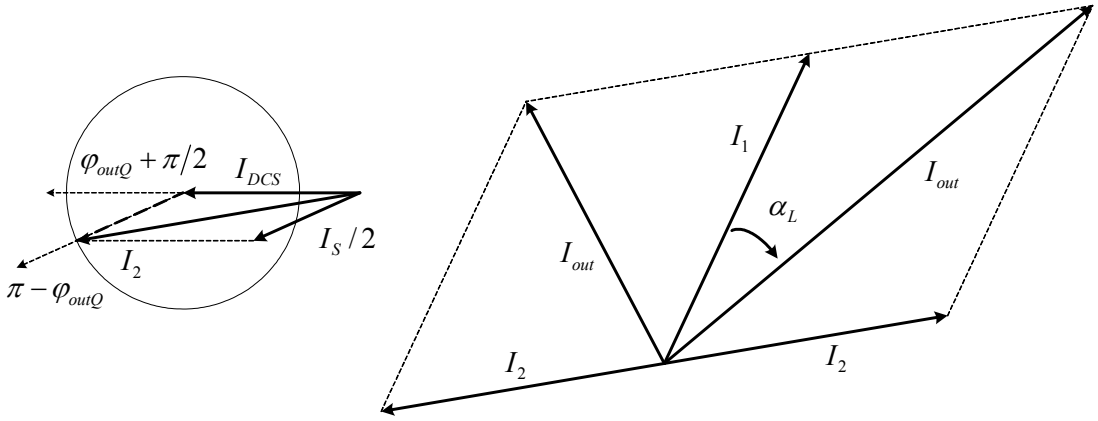
Likewise, in order for the divider to operate properly, we need $\alpha_1+\alpha_L+\beta=0$. However, it is difficult to write down the divider range in a mathematic way. Instead, spectreRF simulation can be performed to help the design and better understanding of the IL-divider with quadrature-phase input signals.



(a) Phasor diagram of I_1



(b) Phasor diagram of I_2 and I_{out} when finQ leads finI by 90°



(c) Phasor diagram of I_2 and I_{out} when finQ lags finI by 90°

Fig. 4.21 phasor diagram plots of the output currents for all cases

One design of the IL-divider with quadrature input signals has been fabricated for demonstration purpose. Fig. 4.22 shows the die photo of the QIIL-divider, which is designed and fabricated in TSMC 0.18-μm CMOS process with 6 metal layers. A quadrature VCO is included to provide the quadrature signals to drive the QIIL-divider. An on-chip SSB mixer is included as well, to measure the sideband rejection of the quadrature signals at divider output. The quadrature-coupled part (Ms, Msc) and differential-coupled part (Ml, Mlc) are designed to have equal size to balance the IQ capacitive loading to the QVCO.

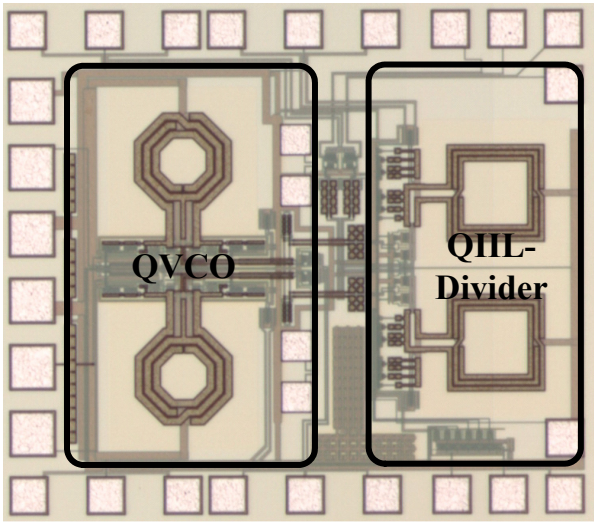
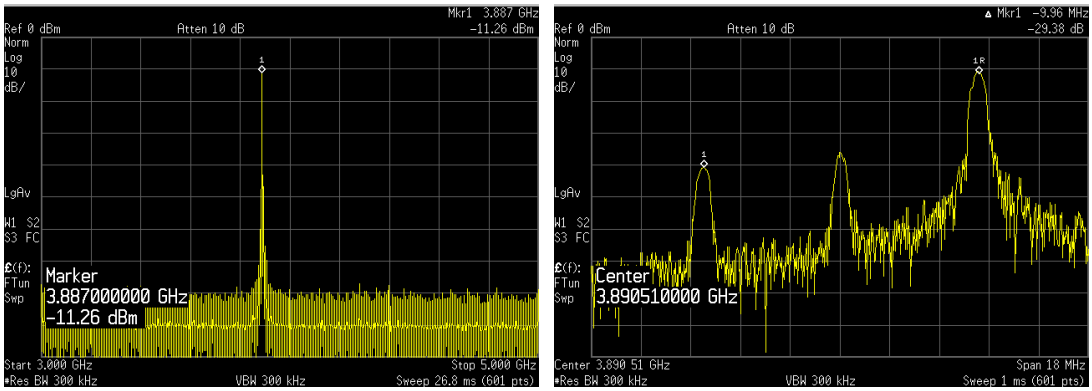


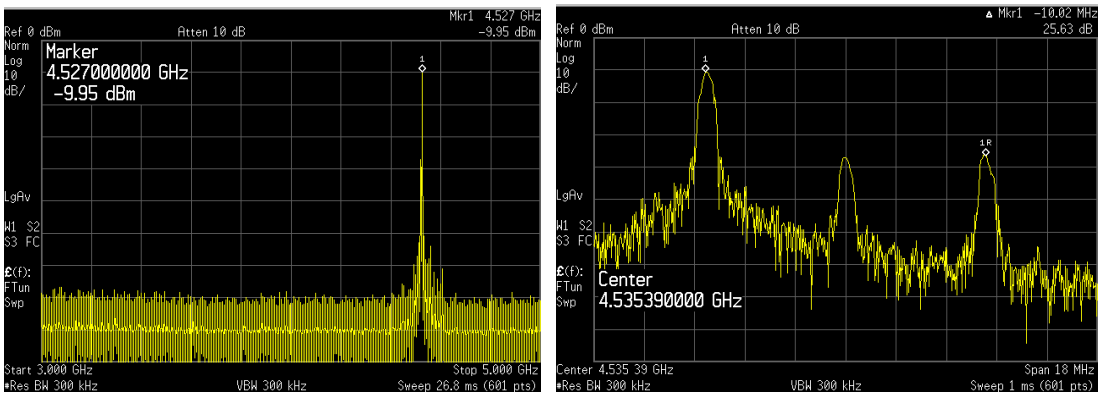
Fig. 4.22 Die photo of the QIIL-divider

It is interesting to find that the divider exhibits two possible self-oscillation frequencies, which is often referred as the bimodal oscillation phenomenon [5]. As shown in Fig.4.23, the lower-frequency self-oscillation happens at 3.88 GHz, and measures an upper-sideband output at SSB mixer output. In contrast, the higher-frequency self-oscillation appears at 4.53 GHz, and exhibits a lower-sideband output.



(a) (b)

Fig. 4.23 (a) output spectrum of the divider with a self-oscillation at lower frequency, (b) sideband rejection plot of its quadrature output signals

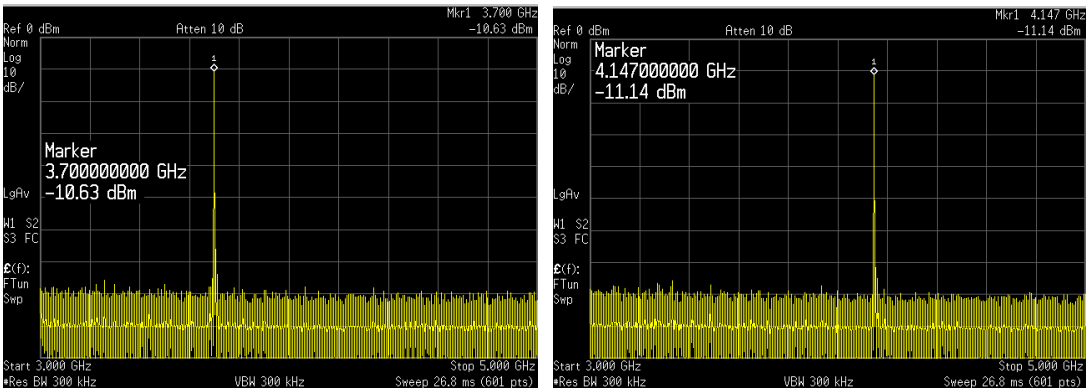


(a) (b)

Fig. 4.24 (a) output spectrum of the divider with a self-oscillation at higher frequency, (b) sideband rejection plot of its quadrature output signals

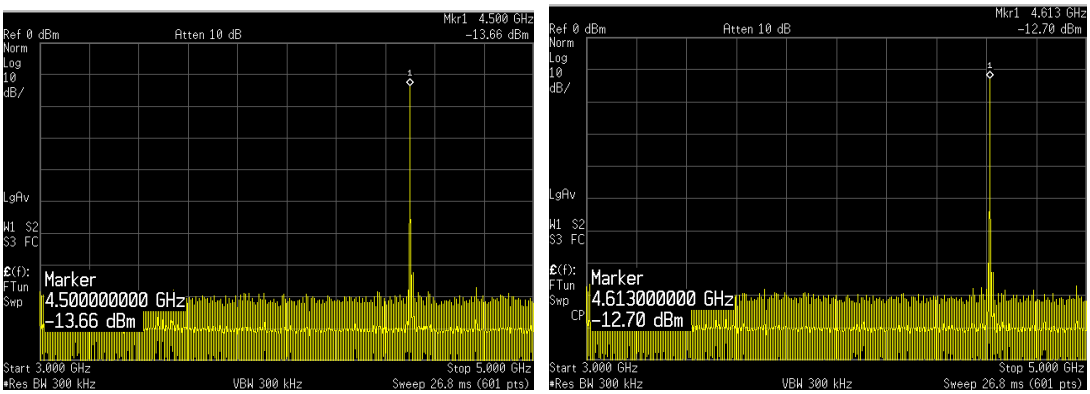
From Fig. 4.23 and Fig. 4.24, we know that the bimodal oscillation signals not only have different output frequencies but also contain opposite output IQ phase sequence. The center frequency of the LC-tank also can be estimated from these two oscillation frequencies, which is located at around 4.2 GHz.

The QVCO in front of the divider is able to cover the output frequency range from 7.2 GHz to 9.74 GHz. However, the QVCO can only provide the quadrature signals with a fixed output IQ phase sequence. The QIIL-divider is measured to have two discontinuous input locking ranges: from 7.4 GHz to 8.3 GHz and from 9 GHz to 9.22 GHz. Fig. 4.25 and Fig. 4.26 show the output spectrums of the divider at lowest and highest input frequency in locking range I and rang II respectively. Fig. 4.27 plots the sideband rejection of the signals at divider output, which are -28.4 dBc at 4.15 GHz output and -26.1 dBc at 4.61 GHz output. The output phase sequence of the signals within two apart locking ranges are observed to be reversed as well.



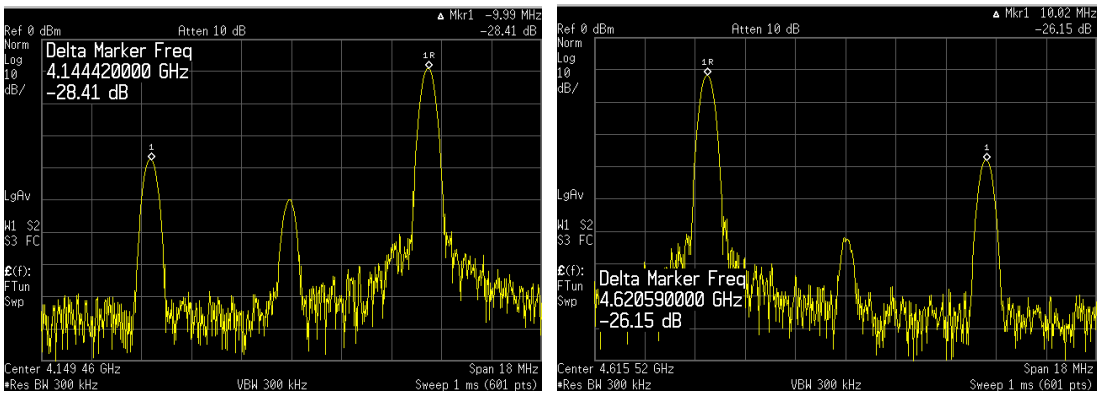
(a) (b)

Fig. 4.25 Output spectrum of the divider at (a) lowest input frequency, (b) highest input frequency in locking rang I



(a) (b)

Fig. 4.26 Output spectrum of the divider at (a) lowest input frequency, (b) highest input frequency in locking rang II



(a) at 4.15 GHz (b) at 4.61 GHz

Fig. 4.27 Sideband rejection plots of the divider output signals

4.3 Regenerative Dividers

4.3.1 Generic Model of Regenerative Dividers

Apart from the injection-locked dividers, regenerative dividers do not have any self-oscillation loops. Consequently, no self-oscillation happens when there is no signal presented at divider input. A typical regenerative (Miller) divider consists of an analog mixer and a feedback loop from the output to the mixer's second input. Fig. 4.28 shows a generic single-loop feedback model of a regenerative divider with both phase shifts in the feedback path and the forward path. Similar to the IL-divider, the three aforementioned conditions are necessary for the divider to operate properly. Assuming that the phase shift introduced by the load is β, the mixer is required to introduce another phase shift α_i so that

$$\alpha_i + \beta + k_1 + k_2 = 0 \tag{4.42}$$

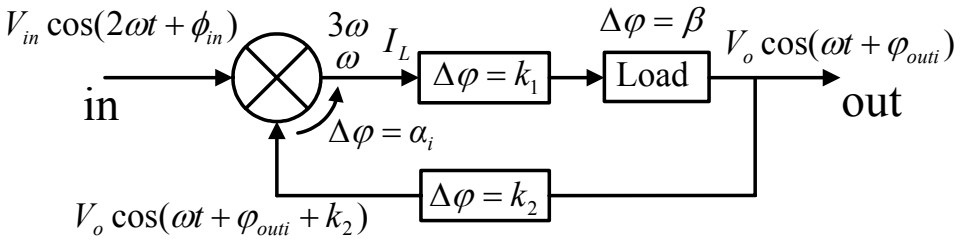


Fig. 4.28 Generic single-loop feedback model of a regenerative divider

For a fully-balanced analog mixer, such as a double-balance Gilbert cell mixer, there are no DC components at the mixer's inputs. Without loss of generality, the input signal can be expressed to be $V_{in}\cos(2\omega t+\phi_{in})$ with an initial phase ϕ_{in}, and the output signal is represented by $V_o\cos(\omega t+\varphi_{outi})$ with an arbitrary output phase φ_{outi}. The mixer output current I_L is derived to be

$$
\begin{aligned}
I_L &= V_{in}\cos(2\omega t+\phi_{in})\times V_o\cos(\omega t+\varphi_{outi}+k_2)\\
&=\frac{1}{2}V_{in}V_o\left[\cos(3\omega t+\phi_{in}+\varphi_{outi}+k_2)+\cos(\omega t+\phi_{in}-\varphi_{outi}-k_2)\right]
\end{aligned}
\tag{4.43}
$$

And the phase shift introduced by the mixer is given by

$$\alpha_i=\phi_{in}-2\varphi_{outi}-2k \tag{4.44}$$

From Eqs. (4.42) and (4.44), the output phase of the regenerative divider is hence given by

$$\varphi_{outi}=\left(\beta+\phi_{in}+k_1-k_2\right)/2 \tag{4.45}$$

4.3.2 Conventional Regenerative (Miller) Divider

Fig. 4.29 shows the schematic of the conventional regenerative divider, in which the output signals are fed-back to the bottom transistors M5~M6 of the mixer. The differential input signals are then applied at switching transistors M1~M4. Likewise, the feedback path and the input signal path can be connected in a swapped way as well.

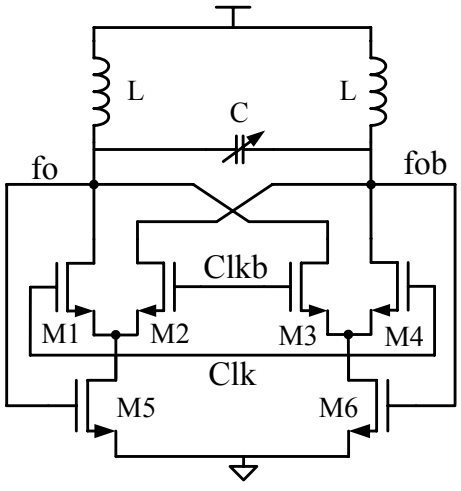


Fig. 4.29 Schematic of the conventional regenerative divider

The single-loop feedback model shown in Fig. 4.29 can be used to analyze the Gilbert cell mixer based regenerative divider with a special case of K_1=0 and K_2=0.

From Eq. (4.44), a fully-balanced analog mixer can compensate for an arbitrarily large phase shift introduced by the load. As a result, the zero phase condition required for a regenerative divider to operate properly can be satisfied automatically. Therefore, regenerative dividers are able to provide a wider operation range than IL-dividers. Although larger power is typically needed because of the cancelled DC component at double-balanced mixer's output.

From Eq. (4.45), it is found that the output phase of a regenerative divider is shifted by 90^o if the input phase is changed by 180^o. By using this characteristic, two identical regenerative dividers driven by swapped differential input signals can be implemented to generate quadrature outputs. The block diagram is illustrated in Fig. 4.30.

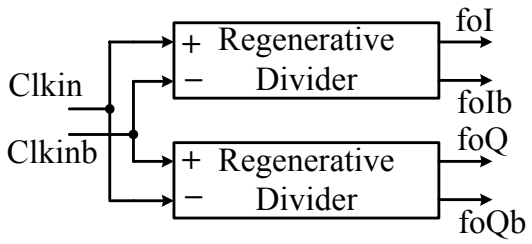


Fig. 4.30 Block diagram of two regenerative dividers for quadrature outputs

4.3.3 Combination of the Regenerative and Injection-locked Divider

In addition to the injection-locked divider shown in Fig. 4.4 and the regenerative divider shown in Fig. 4.29, there is a third kind of the divider topology which is the combination result of the regenerative and the injection-locked dividers. The regenerative-IL divider consists of a fully-balanced analog mixer formed by transistors M1~M6, and a differential-coupled pair constructed by transistors M7~M8. Depending on the transistor size in the differential-coupled pair,

self-oscillation may or may not happen in the regenerative-IL divider. Fig. 4.32 shows the dual-loop feedback model of the regenerative-IL divider for more insight into the operation. In fact, the analysis is similar to the one performed for the conventional IL-divider. It is hence not necessary to repeat again. The transistor sizes of the double-balanced mixer and the differential-coupled pair are determined as the trade-off between the input operation range and the power consumption: larger output current from differential-coupled pair results in the narrower operation rang but lower the total power consumption; Alternately, smaller output current from differential-coupled pair leads to larger size at double-balanced mixer side and hence the increased power consumption but wider input range.

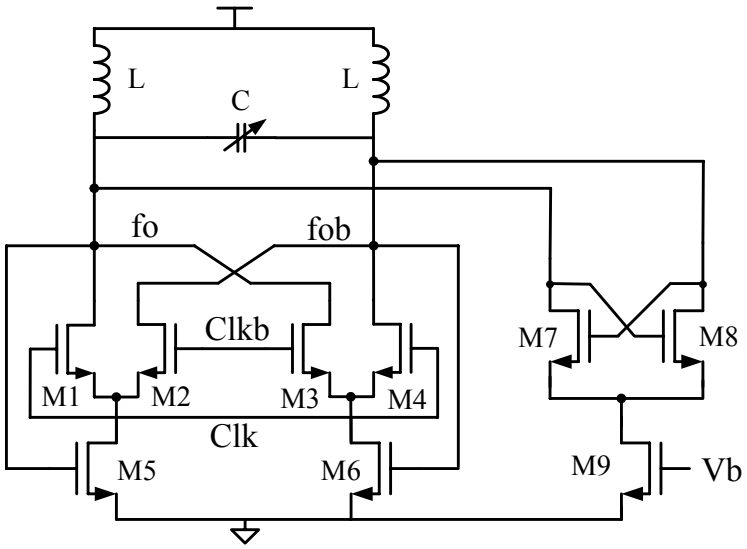


Fig. 4.31 Schematic of the regenerative-IL divider

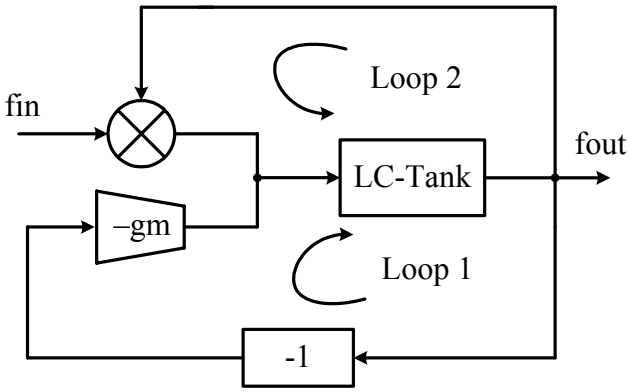


Fig. 4.32 Feedback model of the regenerative-IL divider

4.4 Quadrature-Input Quadrature-Output Regenerative Divider

4.4.1 Motivation

In our MB-OFDM UWB transceiver, quadrature-phase signals are needed not only for in-phase and quadrature-phase mixing in the receiver and transmitter paths, but also for SSB mixing in the synthesizer to generate desired frequencies. SSB mixers require accurate quadrature inputs so as to select the desired signals with high sideband rejection. Basically, as mentioned at beginning, there are two popular ways to implement a quadrature signal generator (QSG) to generate output signals with accurate quadrature phases. The QVCO can be constructed by two cross-coupled LC VCOs to deliver the quadrature phase. Another solution is to use a divide-by-2 divider to achieve the desired frequency and quadrature phase from a VCO operating at a doubled frequency. Many techniques have been previously reported to implement QVCOs or dividers with accurate quadrature outputs [2] [3] [5] [6]. However, the phase matching is still limited in practical applications. One of the critical contributions to the output IQ phase mismatch of a QSG is the mismatch in

its output loading, which typically is dominated by the input capacitive loading of later divide-by-2 divider stage used to divide down the frequency or to achieve additional quadrature signals at a lower frequency.

Fig. 4.33 shows a conventional block diagram of phase-locked loop (PLL) which can be used in UWB synthesizer. Wherein, both QVCO and divide-by-2 dividers are included in the loop to provide the required quadrature phase signals at varied frequencies. There are many types of dividers available, such as source-coupled logic dividers, injection-locked dividers, and regenerative Miller dividers. These existing dividers only employ differential inputs and do not take advantages of quadrature signals available from QSGs. Therefore, as illustrated in Fig. 4.33, dummy dividers are normally included to balance the IQ output loading of the QSG. However, significant capacitive loading mismatch still exists if the dummy dividers were disabled to save power consumption. Alternatively, the dummy dividers could be turned on to improve the IQ loading matching, but that would double the power consumption. In either case, the chip area needs to be doubled due to the dummy dividers.

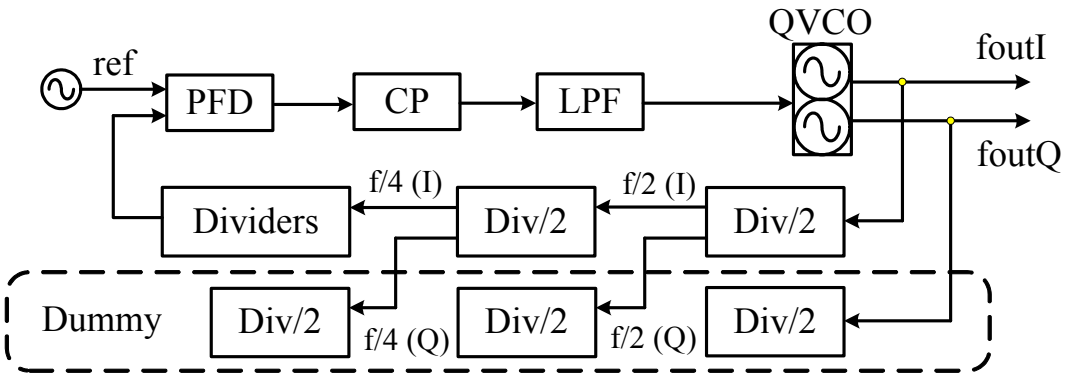


Fig. 4.33 Conventional solution in PLL with dummy dividers for loading matching

Moreover, SSB mixers also require deterministic quadrature phase sequence at the inputs to achieve the correct upper-sideband or lower-sideband operation. However, the output phase sequence of the QVCO is typically ambiguous. Similarly, the quadrature output phase sequence for high-frequency dividers with inductive load is random or depends heavily on the input frequency and the center frequency of the LC tank. Fig. 4.34 shows an example on generating the desired frequency at 3f/2 by SSB mixing. With the uncertainties of the input phase sequence, the SSB mixer may select the wrong sideband frequency of f/2 at the output.

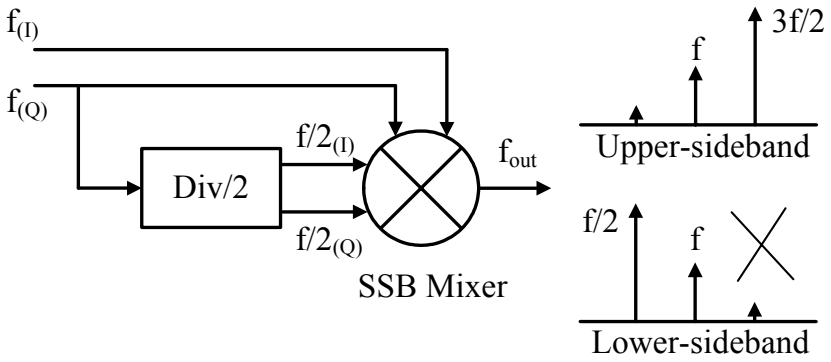


Fig. 4.34 Example of desired frequency generation with SSB mixer

To address all the problems mentioned above, a double-balanced quadrature-input quadrature-output (QIQO) regenerative divider [7] is proposed. As illustrated in Fig. 4.35, with such a proposed QIQO divider, both the input IQ signals from QSG are fully utilized to achieve divide-by-2 operation. Furthermore, such QIQO dividers can be simply cascaded to provide multiple quadrature signals at different frequencies. More importantly, as will be shown later, the proposed QIQO divider can achieve an output IQ phase sequence that is inherently tracked with the input IQ phase sequence. Therefore, compared with the case shown in Fig. 4.44, the relative IQ phase sequence of two SSB mixer's inputs is well determined to deliver

the correct sideband frequency. In other words, the intrinsic quadrature phase sequence of the signals generated by QVCO or other QSGs doesn't need to be studied. In addition, by eliminating the dummy dividers, the proposed solution can have smaller capacitive loading to QSG while simultaneously achieving better IQ loading matching and half of the chip area as well as power consumption. The QIQO divider itself also provides wider operation range and smaller 3rd harmonics.

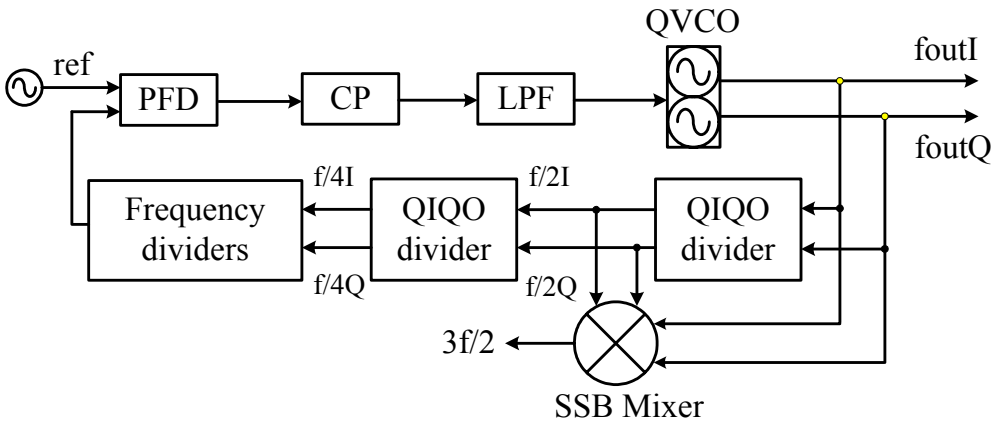


Fig. 4.35 Proposed QIQO divider solution in PLL

4.4.2 Proposed Architecture and Analysis

A simplified block diagram of the proposed QIQO divider is shown in Fig. 4.36, which is based on conventional multiplier-based regenerative (Miller) dividers [8]. However, instead of one feedback loop in conventional Miller dividers, four multipliers and four different feedback loops (Paths 1-4) with appropriate phase shifts are proposed. Both IQ input signals are utilized and applied to Paths 1& 2 and Paths 3 & 4 respectively to achieve divide-by-2 operation. Moreover, Path 1 and Path 3 output currents are added together to form the in-phase output while Path 2 and Path 4 output currents are combined to achieve the quadrature-phase output.

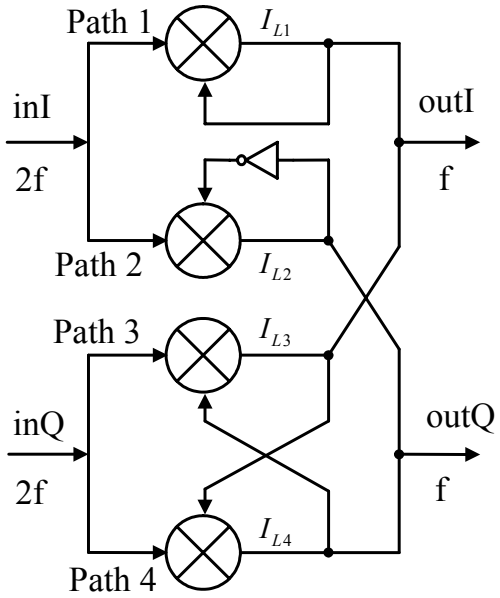


Fig. 4.36 Simplified block diagram of the proposed QIQO divider

Fig. 4.37 shows the behavioral model of a regenerative divider with two paths (Path 1 and Path 2), which is decomposed from the proposed QIQO divider. In Path 1, the output signal is fed-back to the multiplier directly with a zero phase shift. As expressed by Eqs. (4.43) and (4.45), the output current and the output phase of Path 1 are derived as

$$I_{L1} = \frac{1}{2} V_{in} V_o \left[\cos(3\omega t + \phi_{inI} + \varphi_{outI}) + \cos(\omega t + \phi_{inI} - \varphi_{outI})\right] \tag{4.46}$$

$$\varphi_{outI} = (\beta + \varphi_{inI})/2 \tag{4.47}$$

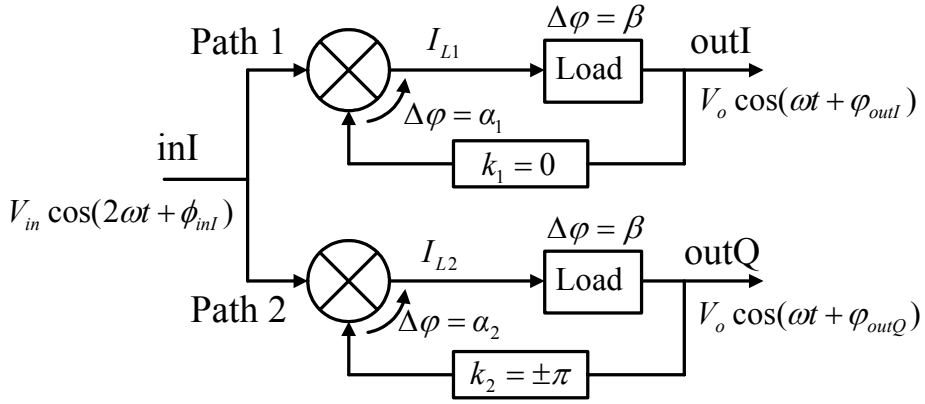


Fig. 4.37 Behavioral model of Path 1 & Path 2

In contrast to Path 1, an 180^o phase shift is intentionally added in the feedback

path of Path 2. However, the phase shift could be either negative or positive 180°, which could cause the output phase in Path 2 either to lead or to lag the output phase in Path 1 by 90°, as expressed in Eq. (4.48)

$$\varphi_{outQ} = (\beta + \varphi_{inI})/2 \pm \pi/2 = \varphi_{outI} \pm \pi/2 \tag{4.48}$$

Consequently, the output current at Path 2 can be re-written as

$$I_{L2} = \frac{1}{2} V_{in} V_o \left[\cos(3\omega t + \phi_{inI} + \varphi_{outI} - \pi/2) + \cos(\omega t + \phi_{inI} - \varphi_{outI} + \pi/2)\right] \tag{4.49}$$

for -180° phase shift in the feedback path or

$$I_{L2} = \frac{1}{2} V_{in} V_o \left[\cos(3\omega t + \phi_{inI} + \varphi_{outI} + \pi/2) + \cos(\omega t + \phi_{inI} - \varphi_{outI} - \pi/2)\right] \tag{4.50}$$

for +180° phase shift in the feedback path.

From Eqs. (4.47) and (4.48), the quadrature outputs are readily achieved and available from the outputs of Path 1 and Path 2 but with uncertain quadrature phase sequence. This is a potential problem in conventional regenerative dividers. However, the problem is completely eliminated in the proposed QIQO divider with the addition of the third and fourth paths that are used to control the phase sequence.

In Path 3 and Path 4, as illustrated in Fig. 4.36, 90° phase shifts are introduced to the feedback paths by making use of the quadrature outputs from Path 1 and Path 2. Fig. 4.38 presents the behavioral model for the in-phase output part of the proposed QIQO divider. The quadrature input signals are represented by $V_{in}\cos(2\omega t + \phi_{inI})$ with initial phase ϕ_{inI} and $V_{in}\cos(2\omega t + \phi_{inQ})$ with initial phase ϕ_{inQ} respectively. The phase shift k_3 in the Path 3 feedback path could be either +90° or -90°, which is dependent on the quadrature output phase sequence of the divider. To determine the quadrature phase sequence of the signals at the inputs and the outputs, it can be

first assumed that the input Q signal (inQ) leads the input I signal (inI) by 90°. That means $\phi_{inQ} = \phi_{inI} + \pi/2$.

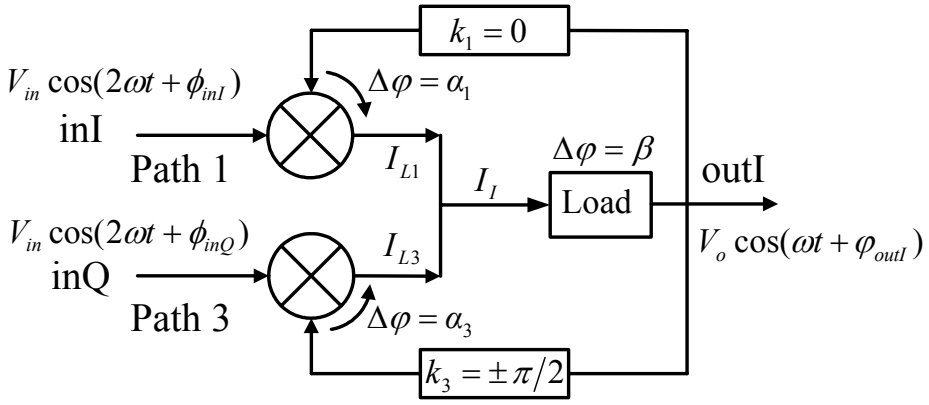


Fig. 4.38 Behavioral model for the in-phase output of the proposed QIQO divider

As one of the two possible scenarios, if the output Q signal lags I signal by 90° ($\varphi_{outQ} = \varphi_{outI} - \pi/2$), the phase shift in the Path 3 feedback loop is - 90°. Therefore, the output current I_{L3} becomes

$$I_{L3} = \frac{1}{2} V_{in} V_o \left[\cos(3\omega t + \phi_{inI} + \varphi_{outI}) + \cos(\omega t + \phi_{inI} - \varphi_{outI} + \pi)\right] \qquad (4.51)$$

Thus, from Eqs. (4.46) and (4.51), the total current I_I becomes

$$I_I = I_{L1} + I_{L3} = V_{in} V_o \cos(3\omega t + \phi_{inI} + \varphi_{outI}) \qquad (4.52)$$

Note that the desired frequency component is automatically cancelled out in this case. As result, the divider loops fail to sustain oscillation.

On the other hand, if the output Q signal leads I signal by 90°, that is $\varphi_{outQ} = \varphi_{outI} + \pi/2$, Eq. (4.51) can be rewritten as

$$I_{L3} = \frac{1}{2} V_{in} V_o \left[\cos(3\omega t + \phi_{inI} + \varphi_{outI} + \pi) + \cos(\omega t + \phi_{inI} - \varphi_{outI})\right] \qquad (4.53)$$

Consequently, Eq. (4.52) is rewritten as

$$I_I = I_{L1} + I_{L3} = V_{in} V_o \cos(\omega t + \phi_{inI} - \varphi_{outI}) \qquad (4.54)$$

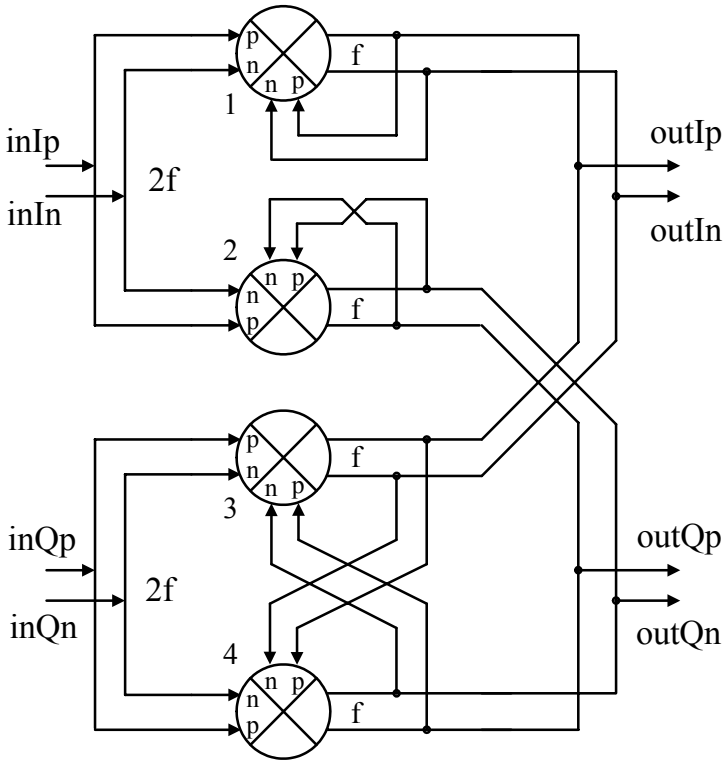
Similarly, the total output currents of Path 2 and Path 4 becomes

$$I_Q = I_{L2} + I_{L4} = V_{in}V_o \cos(\omega t + \phi_{inI} - \varphi_{outI} + \pi/2) \tag{4.55}$$

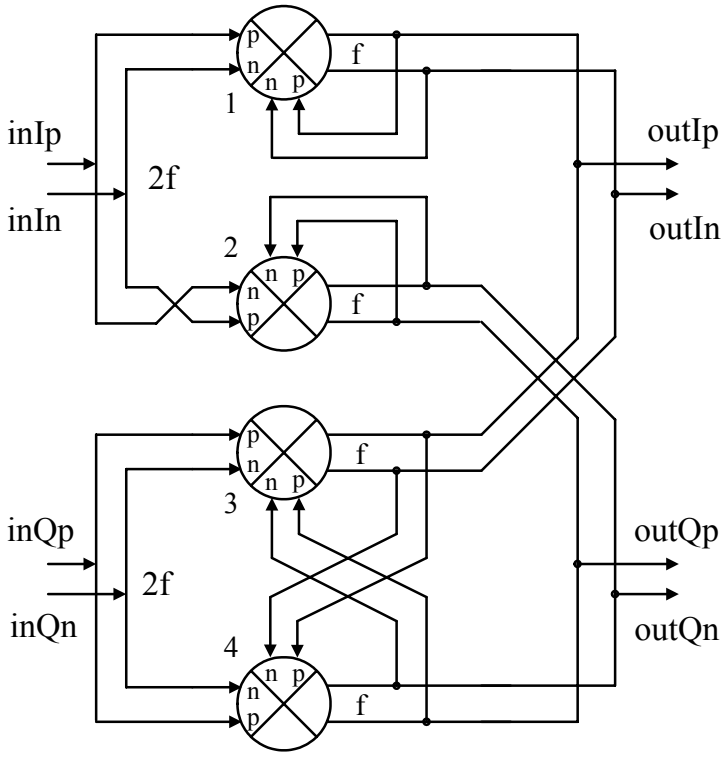
In this case, the divider loops have maximum gain to regenerate and to sustain the oscillation frequency at ω, which forces the Q signal to lead the I signal by 90°.

From above analysis, it can be concluded that if the input Q signal (inQ) leads the input I signal (inI) by 90° ($\phi_{inQ} = \phi_{inI} + \pi/2$), the output Q signal will lead the output I signal by 90°. Similarly, if the input Q signal (inQ) lags the input I signal (inI) by 90° ($\phi_{inQ} = \phi_{inI} - \pi/2$), the output Q signal will also lag the output I signal by 90°. In other words, the IQ phase sequence of the outputs is inherently tracking the IQ phase sequence of the input signals.

The differential configurations of the proposed QIQO divider are illustrated in Fig. 4.39. As shown in Fig. 4.39(a), in Path 1, the output signals are fed-back to the multiplier's second inputs directly. In Path 2, the differential feedback paths are swapped to provide the required 180° phase shift. Alternatively, Path 2 can maintain the same feedback loops as Path 1, but it would need to swap the differential input paths to generate the quadrature phase shift at the output, as explained in Fig. 4.39(b). In Path 3 and Path 4, the multiplier's outputs are cross-coupled and fed-back to the inputs to provide 90° phase shift.



(a) Swapped differential feedback paths at Path 2



(b) Swapped differential input paths at Path 2

Fig. 4.39 Differential block diagram of the proposed QIQO divider

4.4.3 QIQO Divider With Inductive Load

One of the proposed QIQO dividers with inductive load is embedded in our UWB frequency synthesizer described in Chapter 3. Fig. 4.40 shows the block diagram of the fixed-frequency phase-locked loop used in the synthesizer, in which the proposed QIQO divider is driven by a QVCO. In fact, the divide-by-2 dividers in later stages can be replaced with the proposed QIQO divider as well. Nevertheless, for verification purpose, only the first stage divider is implemented.

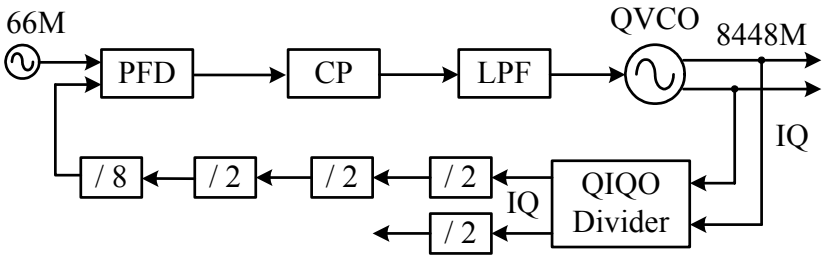


Fig. 4.40 Block diagram of the PLL with proposed QIQO divider

The detailed schematic of the proposed QIQO divider with inductive load is shown in Fig. 4.41. The divider consists of 4 classical Gilbert cell mixers with differential and quadrature input signals. The divider's output signals are fed-back to the switching pairs of the mixers M5-20 rather than to the bottom RF transistors M1-4. This arrangement can reduce the loading capacitance to the previous QVCO stage, which needs to operate at a doubled frequency. Moreover, the eight input RF transistors at the bottom are combined into 4 for better IQ phase balance. Here, the LC tank is chosen to achieve high-frequency operation.

Compared with conventional Miller dividers driven by differential signals, such as the design presented in [3], the overall transistor size as well as the chip area of the QIQO divider is unchanged. Likewise, the power consumption is equal. In

contrast, the conventional design is reconfigured to the proposed topology shown in Fig. 4.41. Consequently, the size of each input transistor in the proposed divider is reduced by half, which significant reduces the capacitive loading to the QVCO and enhances the QVCO loading matching. Furthermore, as mentioned in previous section, an identical dummy divider is avoided. That not only saves the power consumption but also reduces the chip area by half, which are dissipated by the identical dummy divider in the conventional solution shown in Fig. 4.34.

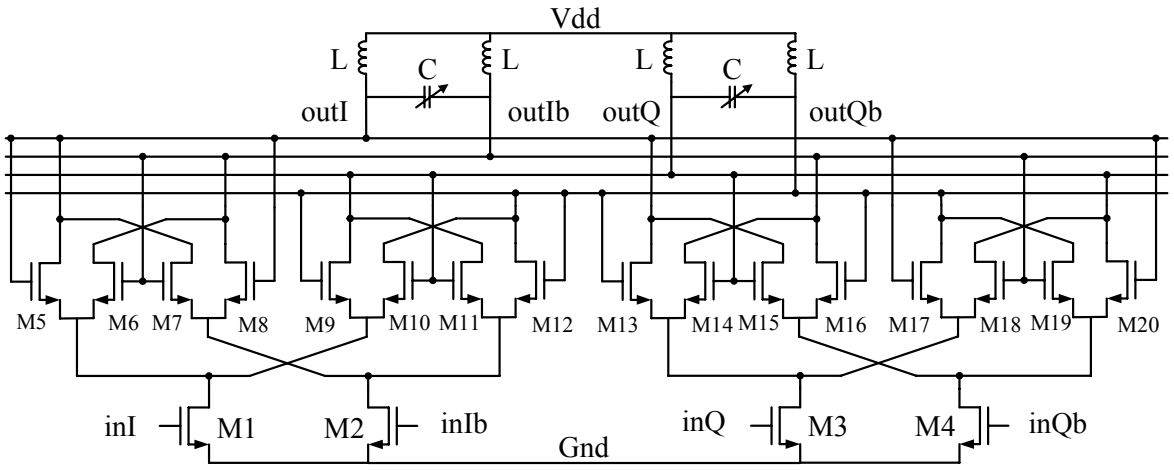


Fig. 4.41 Schematic of the proposed QIQO divider with feedback to switching pairs

4.4.4 QIQO Divider With Resistive Load

In general, resistive load can also be implemented for low frequency and wideband operation since the 3rd harmonics are already suppressed. To further demonstrate this feature, especially to demonstrate the output-input IQ phase sequence tracking feature at the same time, the second divider prototype is implemented, which consists of a cascade of two proposed QIQO dividers but with resistive load instead of inductive load. Fig. 4.42 shows the schematic of the first stage QIQO divider with resistor load for wideband and low frequency operation. In

contrast to the one mentioned above, the divider output signals are fed back to the input transistors M1~4 at bottom instead of the switching pairs, and the input signals are applied to the switching pairs of the mixers M5~20. This arrangement reduces the capacitive loading to the QIQO divider itself and thus extends the output bandwidth. The second stage QIQO divider also employs resistors as the load, but has the same configuration as shown in Fig. 4.41 to further reduce the capacitive loading to the first stage QIQO divider which needs to operate at doubled frequency.

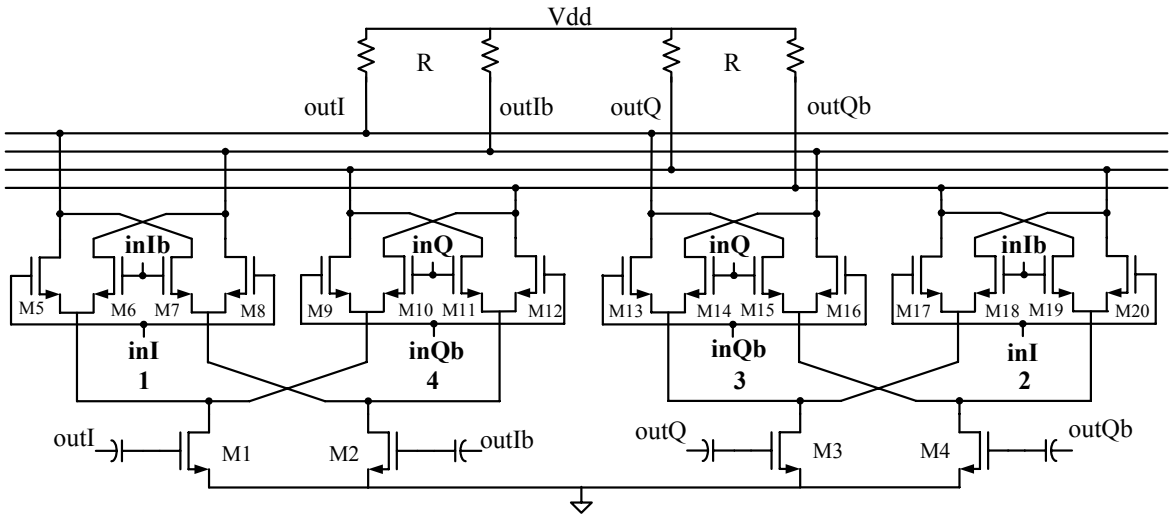


Fig. 4.42 Schematic of the proposed QIQO divider with feedback to bottom transistors

4.4.5 Measurement Results

Both prototypes of the proposed QIQO divider are designed and fabricated in TSMC 0.18-μm CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers. Fig. 4.43 shows the photograph of proposed QIQO divider together with the whole phase-locked loop as illustrated in Fig. 4.40. The proposed QIQO divider with inductive load occupies a chip area of 0.8×0.4 mm^2.

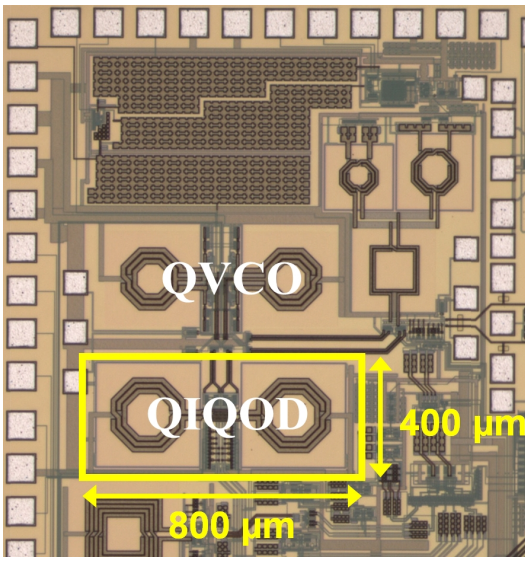
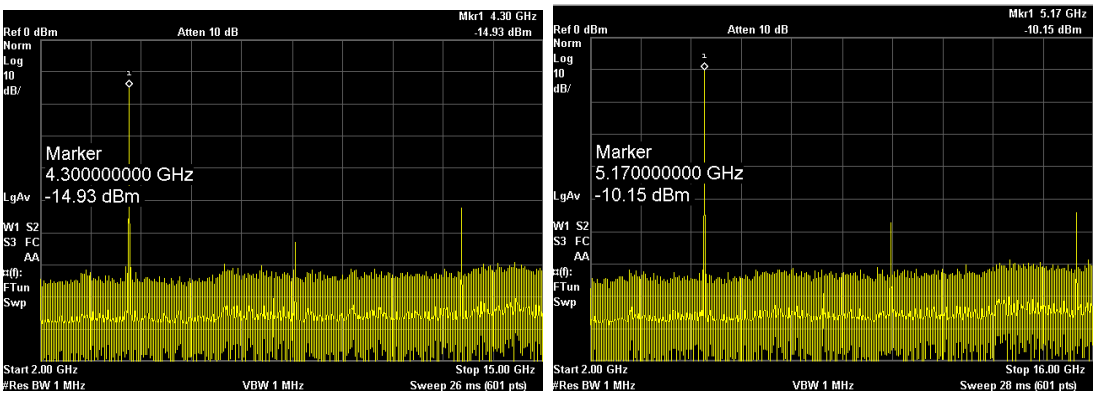


Fig. 4.43 Die photograph of the PLL with proposed QIQO divider for the first design

The Q of the center-tap inductor in the divider is around 8. Fig. 4.44 plots the output spectrums of the QIQO divider in the first design at the minimum and maximum input frequencies with third-harmonic suppression of more than -40 dBc. Due to the limitation of the frequency tuning range of the QVCO, only 18.4% operation bandwidth was measured. At a 0.9-V supply voltage, the QIQO divider consumes a total current from 7.8 mA to 8.7 mA as the input frequency varies from 8.6 GHz to 10.34 GHz.



(a) 4.3 GHz output (b) 5.17 GHz output

Fig. 4.44 Measured output spectrum of the proposed QIQO divider in the first design

To verify the noise contribution of the QIQO divider, the phase noise at both QVCO output and QIQO divider output are measured with close loop measurement in the phase-locked loop system illustrated in Fig. 4.40. Fig. 4.45 compares the measured phase noise at QVCO and QIQO divider outputs. As expected, the phase noise at QIQO divider output is about 6 dB lower than the QVCO output.

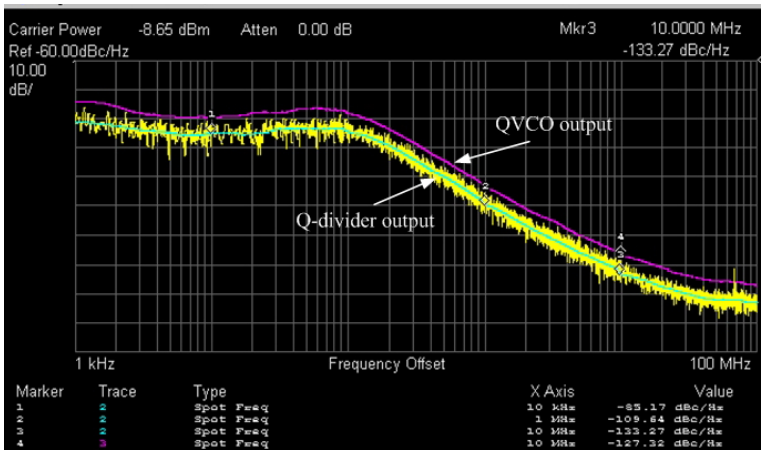
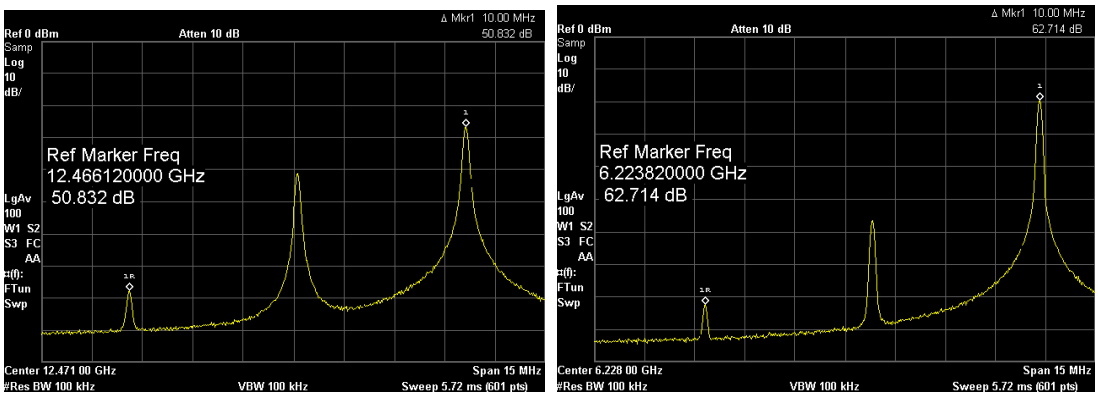


Fig. 4.45 Measured phase noise at QVCO and QIQO divider outputs of the first design

To measure the quadrature phase accuracy of the signals at QVCO output and QIQO divider output, a separate testing structure with the same QVCO and QIQO divider in the first design is also fabricated, which operates at higher frequency because of the smaller loading. Two on-chip SSB mixers are included to measure the image rejection, which are driven by the QVCO and QIQO divider output signals respectively. Agilent E4438C vector signal generator is used to generate the IQ baseband signals at 5 MHz. An image rejection of -50 dBc is measured at the QVCO outputs, and an image rejection of -62 dBc is observed at divider outputs as shown in Fig. 4.46.



(a) QVCO output (b) QIQO divider output

Fig. 4.46 Measured image rejection plots at QVCO and QIQO divider outputs of the first design

The output-input IQ phase sequence tracking feature of the proposed QIQO divider is measured and demonstrated in the second prototype with two cascaded QIQO dividers. Fig. 4.47 shows the testing setup for the second divider prototype. On-chip QVCO and SSB mixer are included to verify and to demonstrate the controllability of the quadrature output phase sequence of the QIQO dividers. The QVCO oscillates at 8.5 GHz with a fixed quadrature phase sequence at output, which dominates the sideband rejection of the SSB mixer (The QVCO has different architecture with the one in aforementioned testing structure.). Fig. 4.48 plots the measured output spectrum at SSB mixer output with an input frequency of 2.9 GHz and a 1.8-V supply. As expected, the SSB mixer is able to jump from lower-sideband to upper-sideband output as the divider's input IQ phase sequence swapped. This measurement proves that the output IQ phase sequence of the proposed QIQO divider is indeed inherently tracked with the input IQ phase sequence.

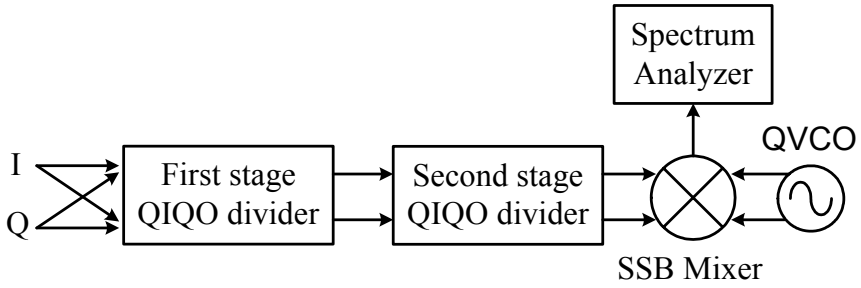


Fig. 4.47 Testing setup for the second divider prototype

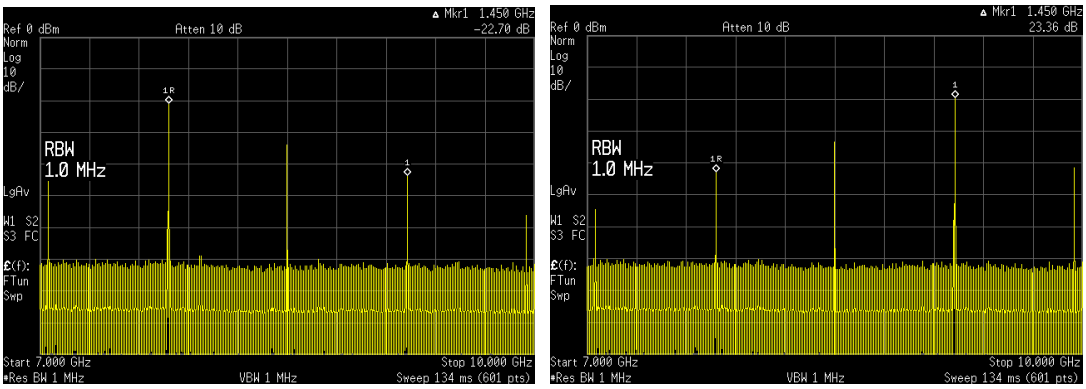


Fig. 4.48 Measured output spectrum of the second prototype with swapped IQ phase sequence at QIQO divider input

4.5 Switchable-IQ-Phase-Sequence Divider Chain

4.5.1 Motivation

SSB mixers are widely used in frequency synthesizers for UWB transceivers to generate required LO signals with fast switching time of less than 9ns. These SSB mixers require second input signals with deterministic and switchable IQ phase sequence (IQPS) to obtain the correct upper or lower-sideband output. Typically, dividers are used to generate the desired second inputs of the SSB mixer. However, the IQPS of the signals generated by conventional dividers can not be switched. IQ multiplexer is used to select the appropriate IQPS of signals at SSB mixer inputs. However, the additional multiplexer needs to consume extra large power, especially

when high frequency signals are presented. To avoid the need of the additional IQ multiplexer for SSB mixer, a divider technique with switchable output IQPS is presented.

4.5.2 Divider Chain Architecture

Fig. 4.49 shows the block diagram of the proposed fast sideband switching SSB mixer which contains dividers with switchable output IQPS.

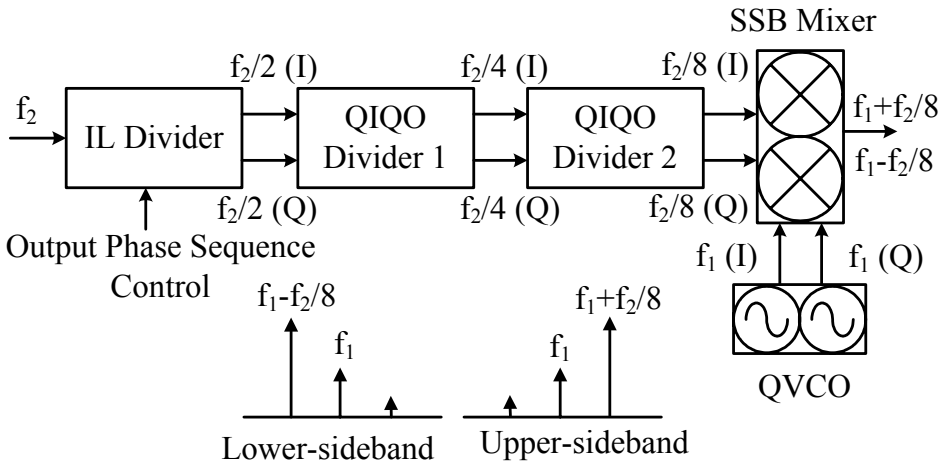


Fig. 4.49 Block diagram of the proposed fast sideband switching scheme

For the 1st stage divider, a DIIL-divider is implemented with one control bit to deterministically switch its output IQPS. The 2nd and 3rd divider are QIQO dividers proposed in section 4.4.4, with the ability of IQPS tracking between the IQ inputs and IQ outputs. Consequently, the required IQPS from DIIL-divider can be obtained at the SSB mixer's input. For demonstration purpose, a transformer-coupled quadrature VCO as proposed in [9] is employed to generate the fundamental quadrature signals with fixed IQPS as the other input of the SSB mixer.

Fig. 4.50 shows the schematic of the DIIL-divider with switchable IQPS at output. The IQPS is chosen by the output frequency (ω_{out}) and the center frequency

of the LC tank (ω_0). As analyzed in section 4.2.3, when ω_{out} lower than ω_0, the output I signal leads Q signal by 90°, and vice versa, when ω_{out} higher than ω_0, the output I signal lags Q signal by 90°. As shown in Fig. 4.50, a variable capacitor C2 is used to tune the center frequency of the LC tank, and a one-bit switched-capacitor C1 is implemented and controlled by FSS to switch the IQPS at the output by making $\omega_{on}<\omega_{out}<\omega_{off}$. Here, ω_{on} and ω_{off} represent the center frequencies of the LC tank when FSS is ON and OFF, respectively.

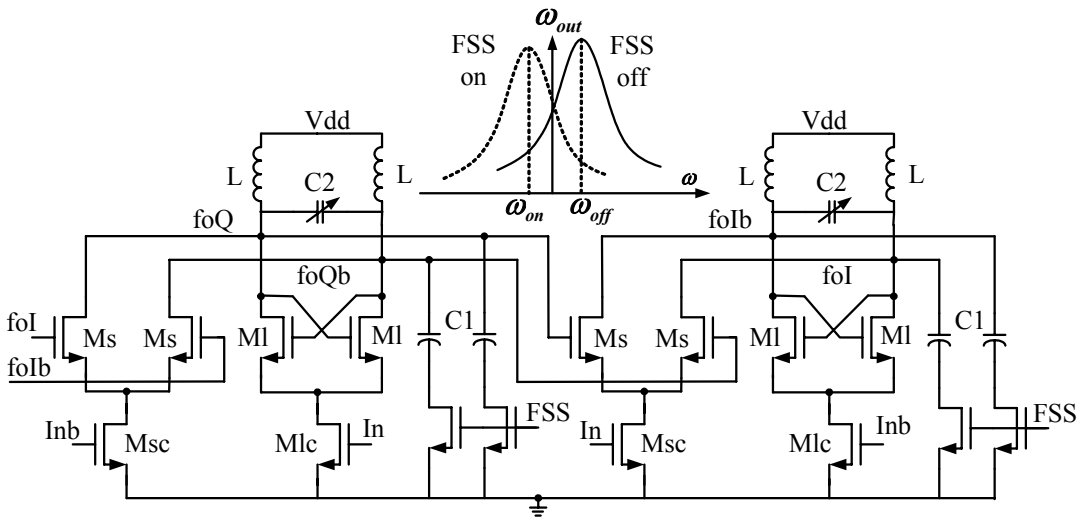


Fig. 4.50 Schematic of the DIIL-divider with switched IQPS

4.5.3 Measurement Results

The proposed IQPS switched divider chain for SSB mixers is designed and fabricated in TSMC 0.18-μm CMOS process with 6 metal layers. Fig. 4.51 shows the die photograph, which occupies the area of 1.3×0.9 mm^2. Operated under 1.8-V supply**,** the dividers consume 10 mA, while the QVCO draws 10 mA at 8.5GHz. To demonstrate the IQ phase switching, the phase sequence control FSS in the IL divider is turned on and off, and Fig. 4.52 plots the corresponding output spectra of the SSB mixer showing correct upper and lower-sideband operations. The measured upper

and lower-sideband rejections are -21.8 dBc and -23 dBc respectively. The input frequency of the divider chain is measured to be from 4.68 GHz to 5.85 GHz, which corresponds to a 22.2% locking range.

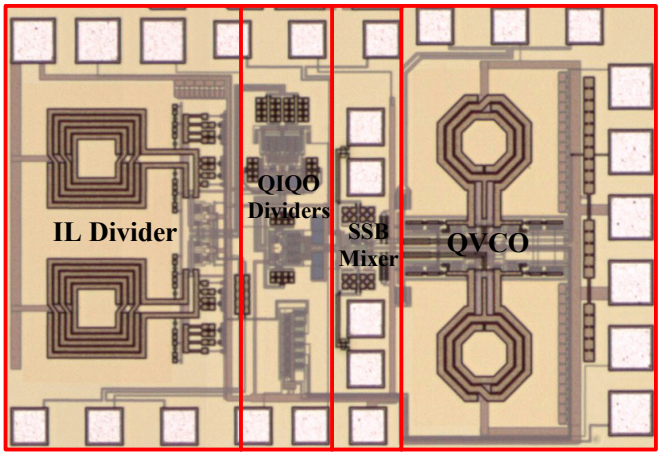


Fig. 4.51 Chip photograph of the proposed IQPS switched divider chain

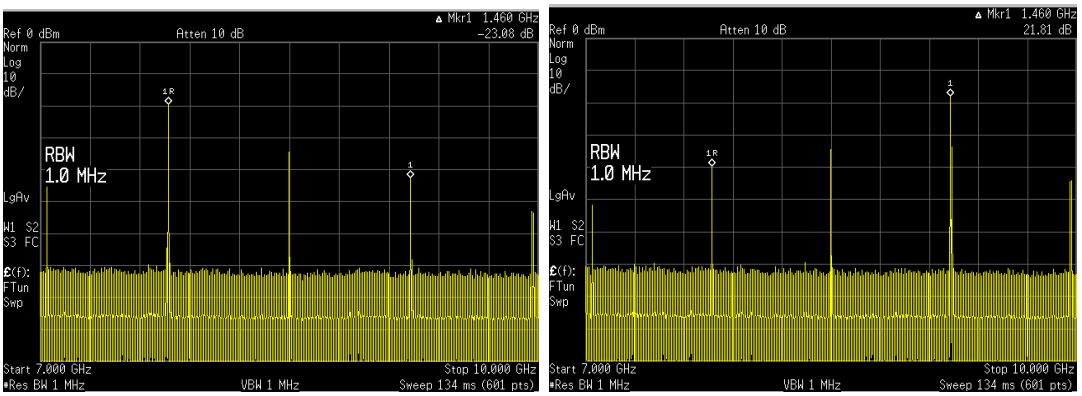


Fig. 4.52 Measured output spectrum of SSB mixer at 5.85 GHz input with FSS on/off

4.6 Ultra-Low-Voltage Divider Using Transformer

As two examples shown in Fig. 4.4 and Fig. 4.29, all the existing dividers require at least two levels of transistors in cascode, which limits the minimum supply voltage to around 1V. To lower the required supply voltage and to reduce the power consumption, a novel IL-divider topology with transformer feedback and a novel transformer-coupled (TC) divider with quadrature outputs are proposed.

4.6.1 ULV Divider With Transformer Feedback

The proposed ultra-low-voltage (ULV) IL divider realize a transformer-feedback VCO and a double-balanced active mixer with transformer-feedback in a stand CMOS process, and features ultra-low supply voltage operation comparable to the device's threshold voltage. Similar with Miller dividers, the proposed ULV-IL divider also provides fully-balanced differential inputs and differential outputs.

Fig. 4.53 shows the schematic of the proposed ULV-IL divider with transformer feedback (TF). The divider includes a TF-VCO as proposed in [10], which is formed by the cross-coupled transistors M5~M6 and integrated transformers Lp and Ls in place of the inductor in conventional LC-VCOs.

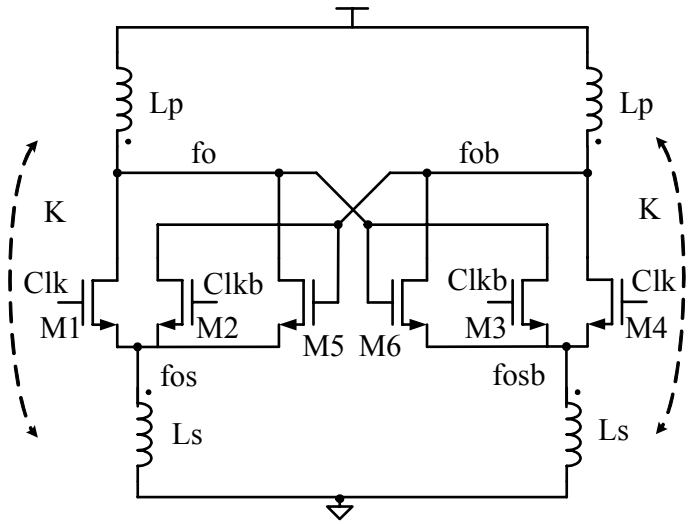


Fig. 4.53 Schematic of proposed ULV-IL divider with transformer feedback

A double-balanced active mixer, constructed by transistors M1~M4 and the same transformer used in VCO, is also implemented with the input clock signals applied at the gate of the switching pair transistors M1~M4. The second coils Ls of the transformers are used to replace the active devices at the bottom of the switching pairs in the conventional Gilbert mixers to achieve low-voltage operation. The output

signals are then coupled back from the primary coils to the secondary coils to serve as the second input of the mixer for the close-loop operation. The divide-by-2 function is finally accomplished by injecting the TF-mixer's output current to the TF-VCO to force the circuit to oscillate at the frequency set by the mixer with transformer feedback loop. With proper transformer coupling, the signals at the drain and the sources can oscillate in phase. In addition, the drain voltage can swing above the supply voltage and the source voltage can swing below the ground potentially. Consequently, the effective minimum supply voltage can be significantly reduced.

Fig. 4.54 illustrates a simplified block diagram of the aforementioned ULV-IL divider, which is constructed by one VCO and one double-balanced mixer with feedback loops. In fact, the proposed divider can still function as a Miller divider without the VCO part for wider operation range but with much larger power. The VCO is included to make the circuit function as an injection-locked divider to achieve good phase noise and low power consumption with compromise in the locking range.

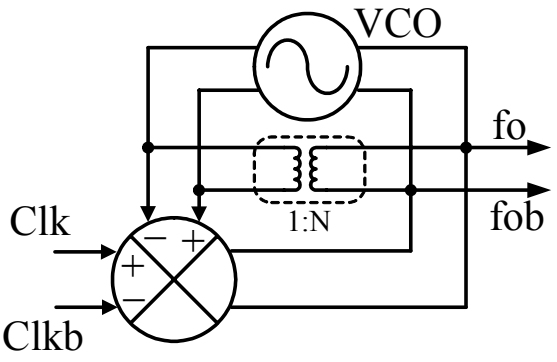


Fig. 4.54 Simplified block diagram of the proposed divider topology

Fig. 4.55 illustrates a dual-loop regenerative model of the proposed ULV-IL

divider. For simplicity, the ideal transformer is assumed with voltage transfer ratio of 1/N (Ls/Lp=1/N). The input transistors M1~M4 are modeled as a double-balanced mixer (Mixer 2). The two inputs of the mixer are the input clock signal at the gate and the signal coupled to the source from the divider's output via transformer feedback, respectively. In addition, there is no DC component presented at the mixer's output since the DC term is canceled by double-balanced inputs. On the other hand, M5~M6 modeled as M1 in Fig. 4.55 can be treated as a single-balanced mixer to multiply with the DC input current. As mentioned previously, the signals at the drain and the source are in phase. With cross-coupled configuration, the gate and source signals become anti-phase, which results in an additional gain of 1+1/N in the feedback path.

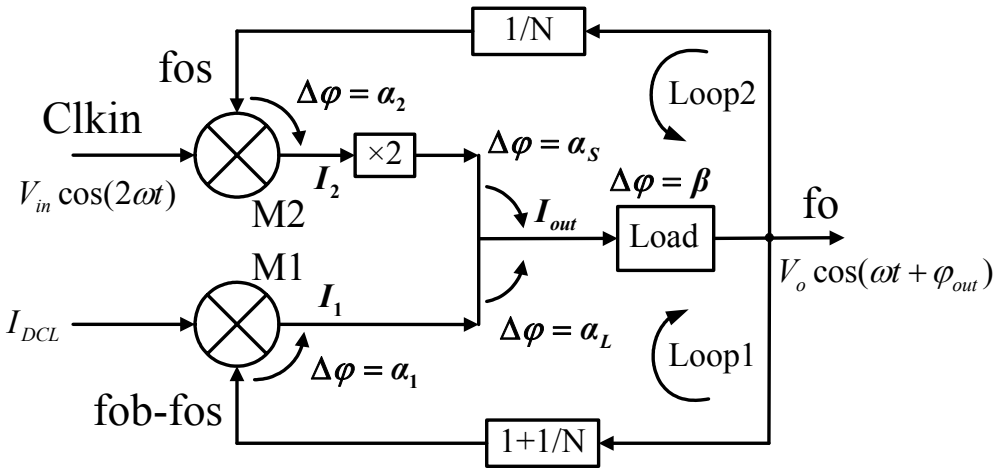


Fig. 4.55 Dual-loop regenerative model of the ULV-IL divider

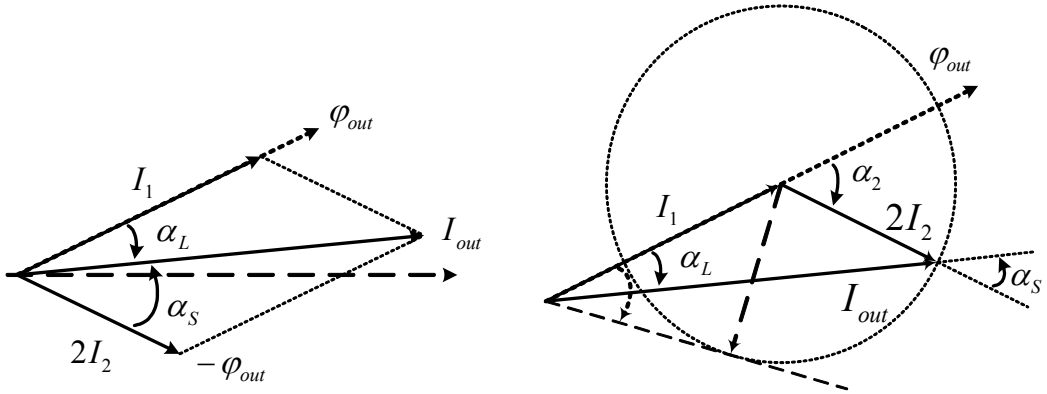
Without loss of generality, the input clock signal can be represented by $V_{in}\cos(2\omega t)$ with an initial phase of zero. The output signal is expressed by $V_o\cos(\omega t + \varphi_{out})$ with an arbitrary phase of φ_{out}. Consequently, the output currents of Mixer 1 and Mixer 2 are expressed by:

$$I_1 = I_{DCL} K_1 (1+1/N) V_o \cos(\omega t + \varphi_{out}) \tag{4.56}$$

$$I_2 = \frac{K_2}{2N} V_{in} V_o \left[\cos(3\omega t + \varphi_{out}) + \cos(\omega t - \varphi_{out})\right] \tag{4.57}$$

Here, K_1 and K_2 denote the conversion gain of the two mixers. Equations (4.56) and (4.57) show that the phase change introduced by Mixer 1 is zero and that the phase shift provided by Mixer 2 is given by $\alpha_2 = -2\varphi_{out}$. In the proposed ULV-IL divider design, $2I_2 < I_1$, and all the related phase shift analysis is done based on this assumption.

To gain better understanding about the phase change around the loops, Fig. 4.56 (a) plots the phasor diagram of the output currents without considering the third-order terms.



(a) (b)

Fig. 4.56 (a) Phasor diagram of the output currents (b) Maximum phase shift of α_L

Note that, in order for the divider to operate properly, the phase shift around the loops must be zero. In Loop 1, $\alpha_1 = 0$, thus we have $\alpha_L + \beta = 0$. That means that the divider needs a phase shift α_L provided by the current summing to compensate for the phase shift β introduced by the load. Given the arbitrary output phase from $-\pi$ to π, as illustrated in Fig. 4.56(b), the maximum phase shift α_L the divider

can provide is calculated as

$$\max(|\alpha_L|) = \arcsin(2I_2/I_1) \tag{4.58}$$

which sets the upper limit of the divider input operation range.

The T-model is used to analyze the integrated transformer in the divider, which is shown in Fig. 4.57. R_L presents the load impedance at second coil. Consequently, the impedance of transformer can be derived as

$$Z_{in} = \frac{j\omega L_p\left[L_s C_s R_L(1-K^2)\omega^2 - j\omega L_s(1-K^2) - R_L\right]}{-L_p C_p L_s C_s R_L(1-K^2)\omega^4 + j\omega^3 L_p C_p L_s(1-K^2) + \omega^2 R_L(L_p C_p + L_s C_s) - j\omega L_s - R_L} \tag{4.59}$$

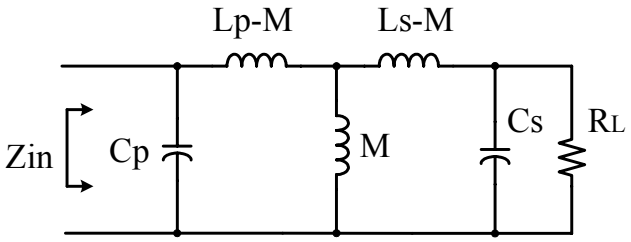


Fig. 4.57 T-Model of the integrated transformer

In the proposed TC-divider, the inductance ratio of the transformer is optimized to be around 4 to optimize the load impedance and the transformer coupling coefficient. As a result, there is only one peak which dominates the load impedance. By defining the quality factor Q of transformer to be the peak frequency over -3dB bandwidth, the impedance can be expressed by

$$Z_{in}(\omega) = Z_{inp}/\left(1 + j2Q(\omega - \omega_p)/\omega_p\right) \tag{4.60}$$

where Z_{inp} and ω_p denote the peak impedance and peak frequency, respectively. Thus, the phase shift induced by transformer is derived as

$$\beta = -\arctan(2Q(\omega - \omega_p)/\omega_p) \tag{4.61}$$

From Equations (4.58) and (4.61), the maximum potential operation range of the divider is hence derived as

$$\Delta\omega/\omega_p = 2I_2\Big/\left(Q\sqrt{I_1^2-(2I_2)^2}\right) \tag{4.62}$$

which is limited by the zero phase shift condition for a regenerative divider to operate successfully. If the other two required conditions are also met, Equation (4.62) also implies that the operation range of the divider can be enlarged by increasing the ratio of the current of the double-balanced mixer part (M1~M4) to that of the VCO part (M5~M6).

To demonstrate the possibility of using the proposed differential IL divider to generate quadrature signals, two of such IL dividers are configured as shown in Fig. 4.58 with differential input signals.

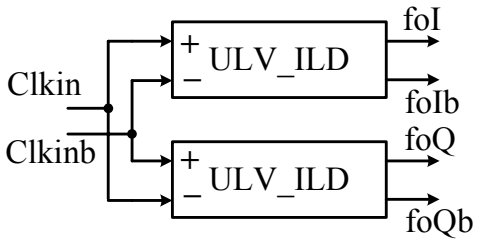


Fig. 4.58 Quadrature generation using the proposed ULV-IL dividers

The dual-loop model, as shown in Fig. 4.55, can be used to study the output phase change at different input phases. Assuming that the input clock signal is expressed by $V_{in}\cos(2\omega t+\phi_{in})$ with an initial phase of ϕ_{in}, the output current of Mixer 2 can be rewritten as:

$$I_2^{"}=\frac{K_2}{2N}V_{in}V_o\left[\cos(3\omega t+\phi_{in}+\varphi_{out}^{"}+\pi)+\cos(\omega t+\phi_{in}-\varphi_{out}^{"})\right] \tag{4.63}$$

The phase shift introduced by Mixer 2 is hence given by $\alpha_2^{"}=\phi_{in}-2\varphi_{out}^{"}$. Meanwhile, under a lock condition, the divider should keep a total zero phase shift in both Loop 1 and Loop 2. As a result, $\alpha_2^{"}=\alpha_2$, and the corresponding output phase

is represented by $\varphi''_{out} = \phi_{in} / 2 + \varphi_{out}$. Therefore, the output phase of the divider will be shifted by 90° if the phase of the input clock signal is changed by 180°. In other words, the desired quadrature output signals generation can be realized by two identical proposed ULV-IL dividers with the two differential inputs swapped.

The proposed ULV-IL divider is designed and fabricated in TSMC 0.18-μm CMOS process (V_{Tn} = 0.52 V, V_{Tp} = - 0.54 V) with 6 metal layers. Fig. 4.59 shows the photograph of two identical ULV-IL dividers as illustrated in Fig. 4.58**,** which occupies a total chip area of 0.97×0.76 mm^2 including all testing pads and a SSB mixer for testing purpose**.** Two 4-port differential center-tap transformers are designed. The single-turn secondary coil of transformer is laid out to be completely inside of the two-turn primary coil. The self-inductances of the primary and secondary coil are measured to be 465 pH and 147 pH, respectively, with a coupling coefficient K of 0.7.

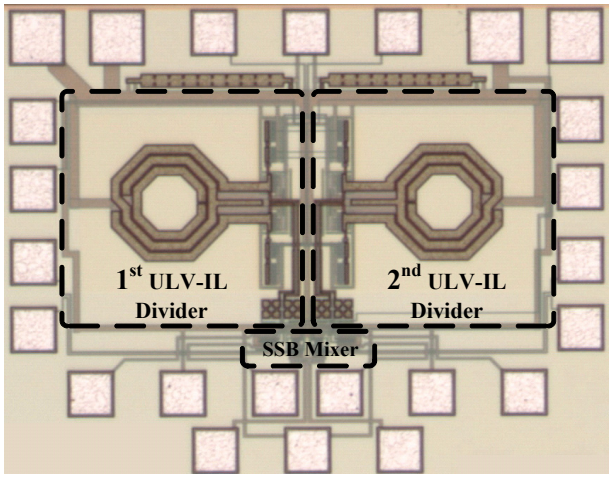
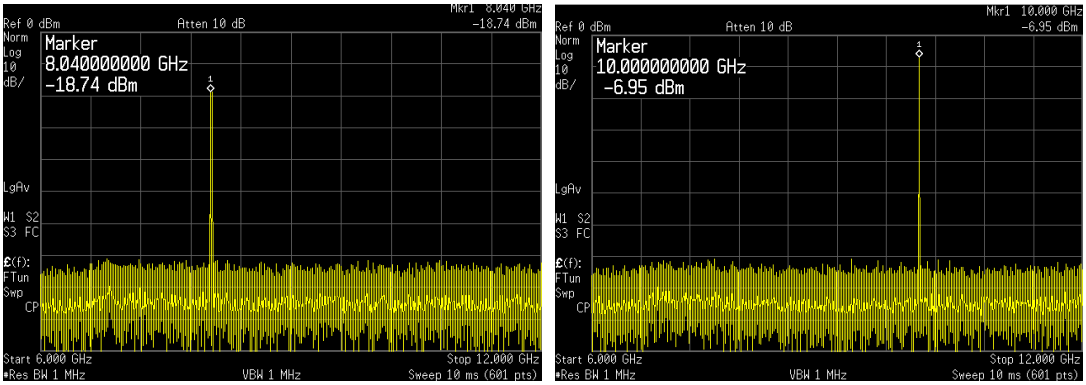


Fig. 4.59 Die photo of the ULV-IL dividers with quadrature outputs

Operated under 0.5-V ultra-low supply voltage, a single divider consumes a total power from 2.75 mW to 4.35 mW as the input frequency varies. An input

frequency range from 16.1 GHz to 20 GHz is measured with 3-bit switched capacitors tuning, which corresponds to 21.6 % range and is actually limited by the maximum frequency of the external power splitter. Fig. 4.60 shows the output spectrums of the proposed ULV-IL divider at the minimum and maximum input frequencies.



(a) 16.1 GHz input (b) 20 GHz input

Fig. 4.60 Measured output spectrum of the proposed ULV-IL divider at (a) Minimum input frequency, (b) Maximum input frequency

Figure 4.61 plots the output power versus input frequency for different power consumption levels by varying the supply voltage to change the current. The common DC input voltage of the input clock signal is biased at its respective supply voltage. The input frequency range associated with minimum power dissipation and supply voltage of 0.5V is limited by the loop gain condition mentioned in the previous section, which thus can be improved by increasing the supply voltage and thus power consumption. On the other hand, the divide range extension is no longer obvious when the power consumption is beyond 8 mW because the zero phase shift condition becomes dominant.

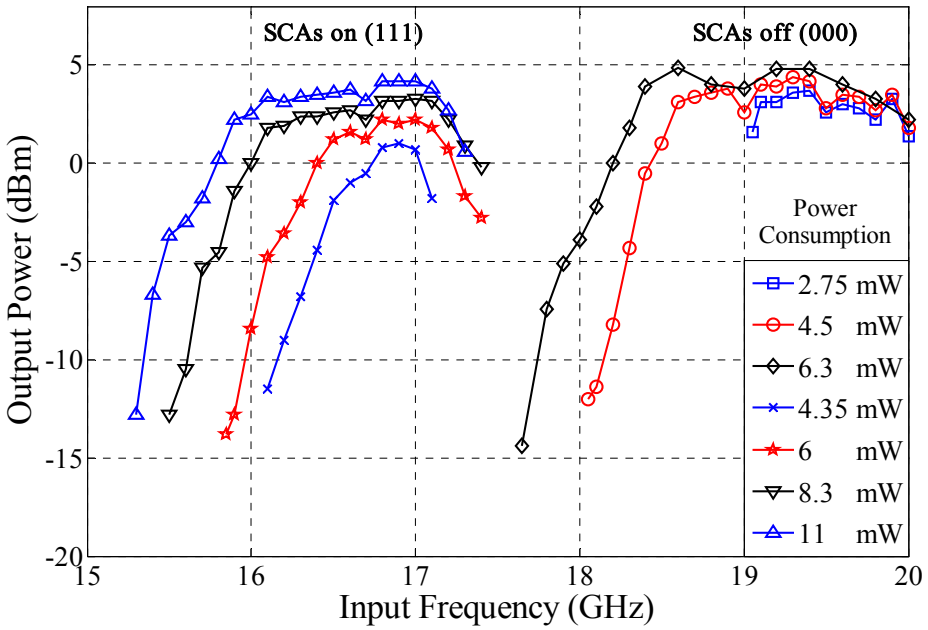


Fig. 4.61 Measured output power vs. input frequency of single divider at different power consumption levels

To verify phase accuracy of the quadrature signals generated by two identical ULV-IL dividers with anti-phase inputs as shown in Fig. 4.58, an on-chip SSB mixer is included to measure the sideband rejection. Again, Agilent E4438C vector signal generator is used to generate the IQ baseband signals at 5 MHz. As shown in Fig. 4.62, sideband rejection of better than -35 dBc is measured, which is actually limited by the phase mismatch of the differential RF input signals.

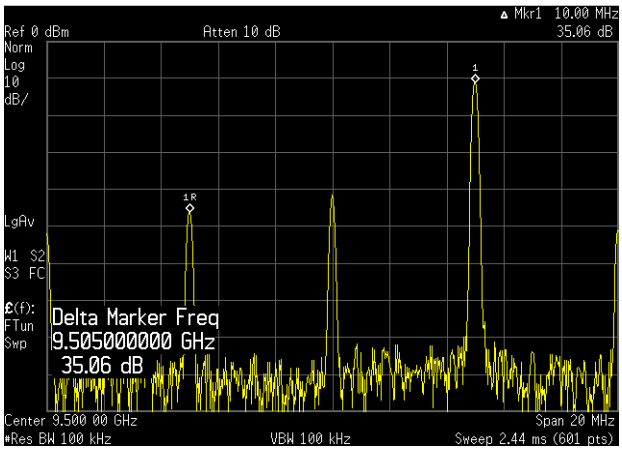


Fig. 4.62 Measured sideband rejection of two ULV-IL dividers with quadrature outputs shown in Fig. 4.58

4.6.2 ULV Divider With Transformer-coupled QVCO

The proposed transformer-coupled (TC) divider employs a transformer-coupled QVCO and two transformer-cross-coupled double-balanced active mixers to enable ultra-low voltage operation while simultaneously achieving wider input frequency range and lower power consumption. Fig. 4.63 illustrates a simplified block diagram of the proposed TC-divider topology for intuitive understanding, which is constructed by one QVCO and two mixers with cross-coupled feedback loops.

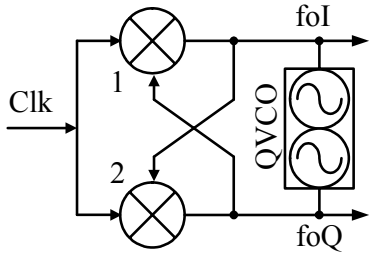


Fig. 4.63 Simplified block diagram of the proposed divider topology

Similar to the operation in injection-locked dividers, the divide-by-2 function of the proposed TC-divider is accomplished by injecting the output current from the double-balanced mixers into QVCO to force it to oscillate at the frequency set by the mixers with cross-coupled feedback loops. A behavioral model of these two mixers with cross-coupled feedback loops is illustrated in Fig. 4.64.

Here, the output phases of Path 1 and Path 2 are assumed to be φ_{out1} and φ_{out2} respectively. From Eq. (4.45), the output phase for Path 1 is calculated as

$$\varphi_{out1} = \beta + \phi_{in} - \varphi_{out2} \tag{4.64}$$

Similarly, we can derive the output phase for Path 2 as:

$$\varphi_{out2} = \beta + \phi_{in} - \varphi_{out1} \tag{4.65}$$

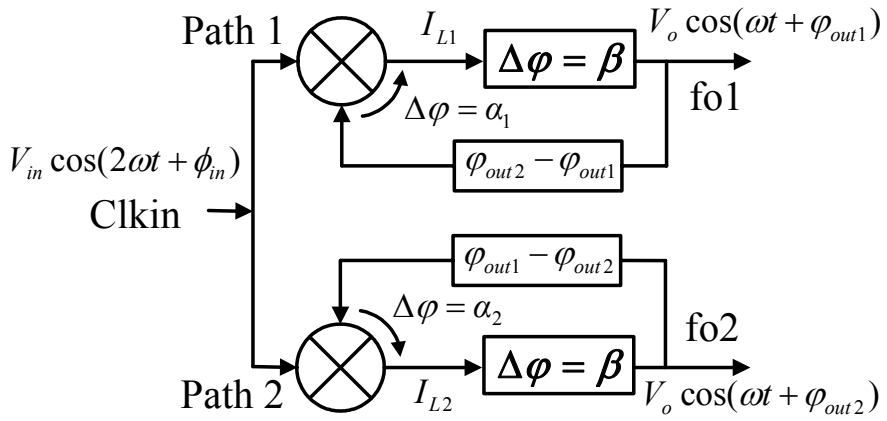


Fig. 4.64 Behavioral block diagram of two cross-coupled mixers

From Eqs. (4.64) and (4.65), the output phases of the two paths can be arbitrarily independent of each other. In other words, the cross-coupled mixer, in fact, can not provide the desired quadrature signals, and the quadrature generation is actually realized by the QVCO.

Fig. 4.65 shows the detailed schematic of the proposed TC-divider with quadrature outputs. The divider contains a TC-QVCO as proposed in [9] and two double-balanced active mixers. The TC-QVCO is configured by two cross-coupled transistor pairs M9~M12 and two integrated transformers. The two VCOs are cross-coupled by on-chip transformers, rather than active devices, to generate quadrature signals with better performance in terms of operation frequency, power, supply voltage, and phase noise [9]. The primary coil of each of the transformer Lp resonates with the total capacitance at the drain and is simultaneously cross-coupled to the secondary coil Ls for quadrature outputs. As such, the loading capacitance contributed by the coupling transistors in conventional QVCO is removed, and the supply voltage can be lower because the transformer enables the signals at the sources to swing below the ground.

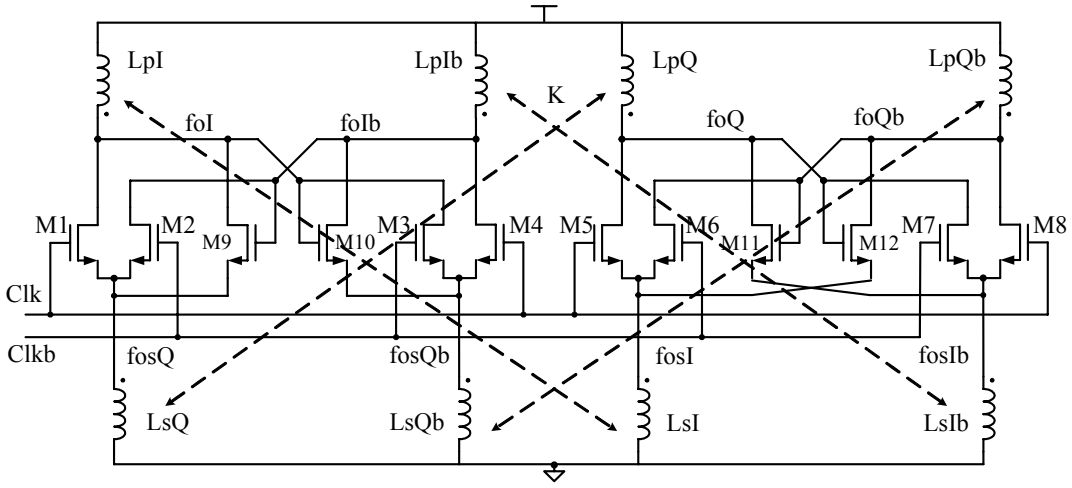


Fig. 4.65 Schematic of proposed TC-divider

Two double-balanced active mixers, constructed by transistors M1~M8 and transformers, are also configured in cross-coupled connection through the same transformers used in the QVCO. The differential input clock signals are applied at the gate of the switching pair transistors M1~M8. The active device at bottom of the switching pairs in conventional Gilbert cell mixer is removed to achieve low-voltage operation. Instead, the second coil Ls of each of the transformer is placed at source terminal of the mixer to realize the second input. The first mixer's output signals are then coupled to the second input of the second mixer through the transformer to form the cross-coupled connections. Thanks to transformer coupling for both the mixer and the VCO, the minimum necessary supply voltage of the proposed TC-divider is significantly reduced.

To fully understand the operation of the proposed TC-divider, the I-output part of the divider is modeled as a dual-loop regenerative divider with two mixers and feedback loops as shown in Fig. 4.66. For simplicity, the ideal transformer is assumed with voltage transfer ratio of 1/N (Ls/Lp=1/N). The input transistors

M1~M4 are modeled as a double-balanced mixer (Mixer 2). The two inputs of the mixer are the input clock signal at the gate and the signal coupling to the source from the Q-output part via transformer. In addition, there is no DC component at the mixer's output since the DC term is canceled by double-balanced inputs. On the other hand, M9~M10 can be treated as a single-balanced mixer to multiply with DC current input and is modeled as M1 in Fig. 4.66. Furthermore, the gate and source voltage signals appear in quadrature phases, which results in the two feedback paths in Loop 1.

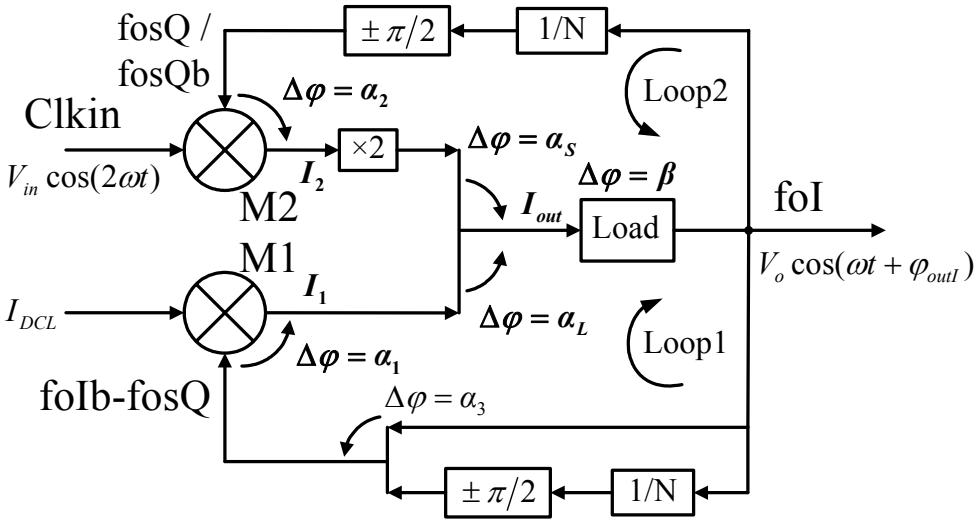


Fig. 4.66 Dual-loop regenerative model of the proposed TC-divider

From the dual-loop model in Fig. 4.66, the I-output signal could be either leads or lags the Q-output signal by 90°. Without loss of generality, the input clock signal can be represented by $V_{in}\cos(2\omega t)$ with initial phase of zero. The I-output signal is expressed by $V_o\cos(\omega t+\varphi_{outI})$ with arbitrary phase of φ_{outI}.

Consequently, the output currents of Mixer 1 and Mixer 2 are expressed by

$$I_1 = I_a + I_b \tag{4.66}$$

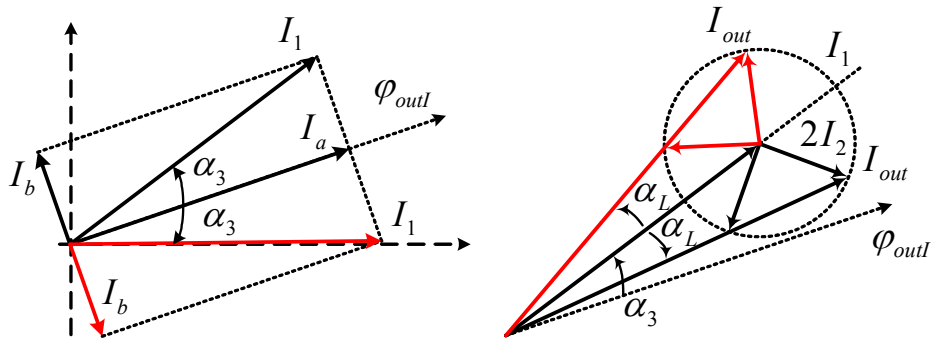
With $I_a = I_{DCL}K_1V_o\cos(\omega t+\varphi_{outI})$ and $I_b = 1/N\, I_{DCL}K_1V_o\cos(\omega t+\varphi_{outI}\pm\pi/2)$

$$I_2 = \frac{K_2}{2N} V_{in} V_o \left[\cos(3\omega t + \varphi_{outI} + \pi/2) + \cos(\omega t - \varphi_{outI} - \pi/2)\right] \tag{4.67}$$

Here, K_1 and K_2 denote the conversion gain of the two mixers. In addition, as shown in Fig. 4.66 and Eq. (4.67), only the $+\pi/2$ or $-\pi/2$ phase shift needs to be considered in Loop 2's feedback path since the arbitrary output phase of φ_{outI} can already cover the opposite case.

Figure 4.67(a) plots the phasor diagram of the output current I_1 in Loop 1. The phase shift provided by Mixer 1 is zero ($\alpha_1 = 0$), and the phase shift in the feedback loop is given by a constant $\alpha_3 = \pm\arctan(1/N)$. In the proposed TC-divider, the AC mixing current in Loop 2 is smaller then DC mixing current in Loop 1, as expressed by $2I_2 < I_1$. Consequently, the phasor diagram of I_{out} and the phase shift α_L introduced by current adding of I_1 and I_2 are illustrated in Fig. 4.67(b). With an arbitrary output phase from $-\pi$ to $+\pi$, the maximum phase shift α_L the divider can provide is calculated as

$$\max(|\alpha_L|) = \arcsin(2I_2/I_1) \tag{4.68}$$



(a) (b)

Fig. 4.67 Phasor diagram of the output currents in Loop 1 of Fig. 4.66

Note that, in order for the divider to operate properly, the phase shift around the loops must be zero. In Loop 1, $\alpha_1 = 0$, thus we have $\alpha_L = -(\alpha_3 + \beta)$. On the

other hand, the divider should always oscillate at the situation which can maximize the output current I_{out} to achieve the largest loop gain. As explained in Fig. 4.67(b), the smaller phase angle α_L means the larger output current I_{out}. Hence, under operation condition, we have

$$|\alpha_L| = \min|(\alpha_3 + \beta)| \tag{4.69}$$

When $\beta>0$, $\alpha_3 = -\arctan(1/N)$, and the divider I-output signal leads Q-output signal by 90^o. Similarly, when $\beta<0$, $\alpha_3 = +\arctan(1/N)$, and the divider I-output signal lags the Q-output signal by 90^o.

From Eq. (4.61), when the divider output frequency ω_{out} is lower than peak frequency ω_p, the phase shift becomes $\alpha_3 + \beta = \beta - \arctan(1/N)$, and the I-output signal leads the Q signal by 90^o. Similarly, when ω_{out} is higher than ω_p, the phase shift becomes $\alpha_3 + \beta = \beta + \arctan(1/N)$, and the I-output signal lags the Q signal by 90^o. Moreover, the divider operation range is enlarged since it can compensate with a wider range of phase shift introduced by the load, which also can be seen from Eqs. (4.68) and (4.68). However, since $\alpha_L + \alpha_3 + \beta = 0$ may not be satisfied when β close to zero, the divider can fail to function at frequencies close to the output peak frequency, which would introduce a gap in the input frequency range.

The proposed TC-divider with quadrature outputs is designed and fabricated in TSMC 0.18-μm CMOS process (V_{Tn} = 0.52 V, V_{Tp} = - 0.54 V) with 6 metal layers. Fig. 4.68 shows the photograph of the TC-divider, which occupies a chip area of 0.97×0.76 mm^2 including all testing pads. Two 4-port differential center-tap transformers, the same design as the one in ULV-IL divider, are used.

Note that, the designed TC-divider has the same device sizes as the previous reported ULV-IL divider in Section 4.61. However, the minimum required supply voltage for the TC-divider is around 100mV higher than the ULV-IL divider. The minimum supply is actually determined by the loop gain of the feedback loop. In the ULV-IL divider, both the transformer feedback loop and the differential-cross-coupled loop contribute the star-up loop gain to the divider. While, in the proposed TC-divider, the transformer coupled loop is utilized to form the required quadrature loop in the divider. As a consequence, that results in the smaller start-up loop gain and higher minimum supply voltage in the TC-divider.

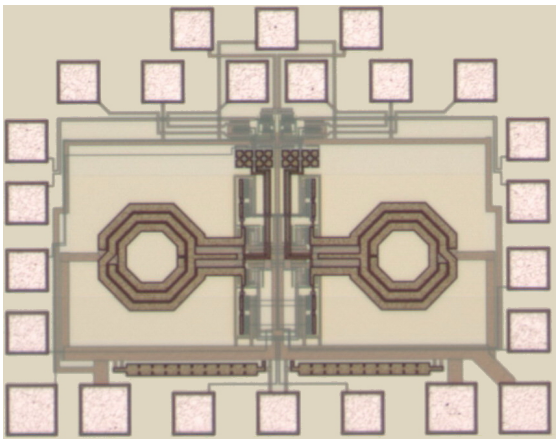
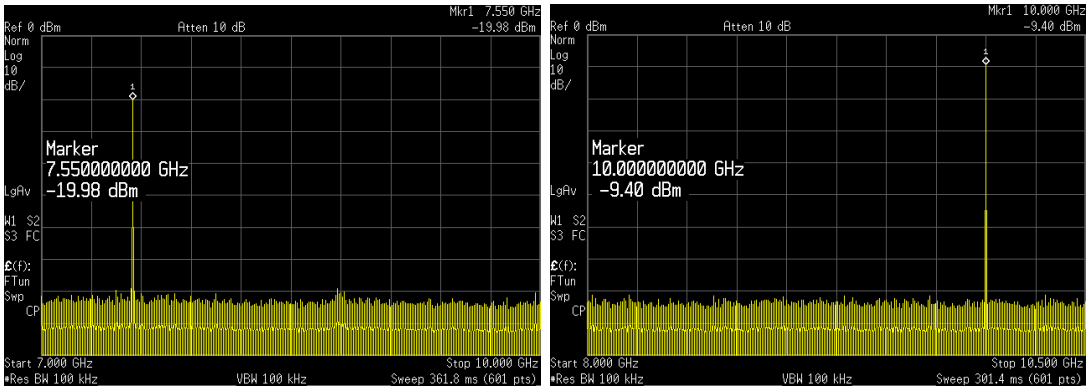


Fig. 4.68 Die photograph of the TC-divider with quadrature outputs

Operated at 0.6-V supply voltage, the divider consumes a total power from 11.4 mW to 13.6 mW as the input frequency varies. An input operation range from 15.1 GHz to 20 GHz is measured with 3-bit switched capacitors tuning, which corresponds to 27.8 % range and is actually limited by the maximum frequency of the external balun. Fig. 4.69 (a) and (b) shows the output spectrums of the proposed TC-divider at the minimum and maximum input frequencies, respectively. The measured output power versus input frequency plots are shown in Fig. 4.70.



(a) (b)

Fig. 4.69 Measured output spectrums of the proposed TC-divider at (a) Minimum input frequency, (b) Maximum input frequency

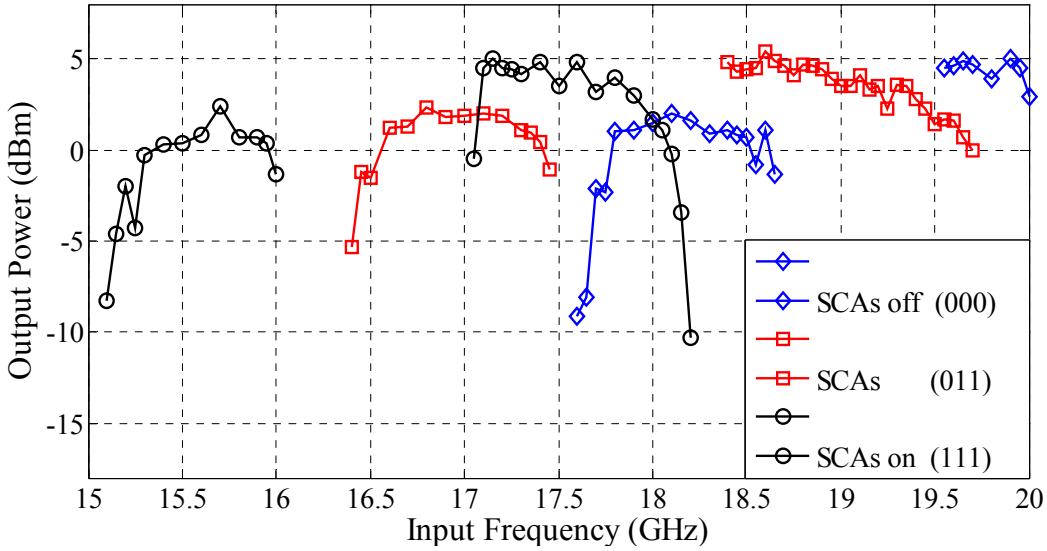


Fig. 4.70 Measured output power vs. input frequency

In addition, a sideband rejection of -31 dBc is measured as shown in Fig. 4.71.

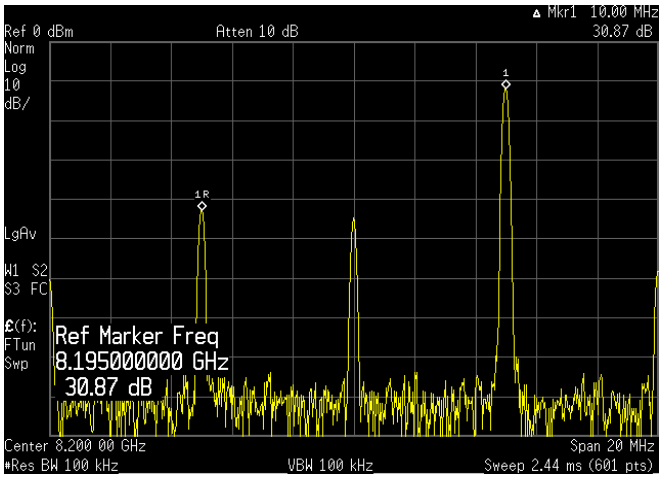


Fig. 4.71 Measured sideband rejection of the TC-divider

As plotted in Fig. 4.72, the sideband rejection and thus the IQ phase accuracy of the divider are degraded at the output frequencies close to the peak frequency of the load, since the QVCO can not provide clearly quadrature phase at this region. As expected, the SSB mixer's output is changed from upper-sideband to lower-sideband when the divider output frequency is swept from lower to higher as compared to the peak frequency of the load.

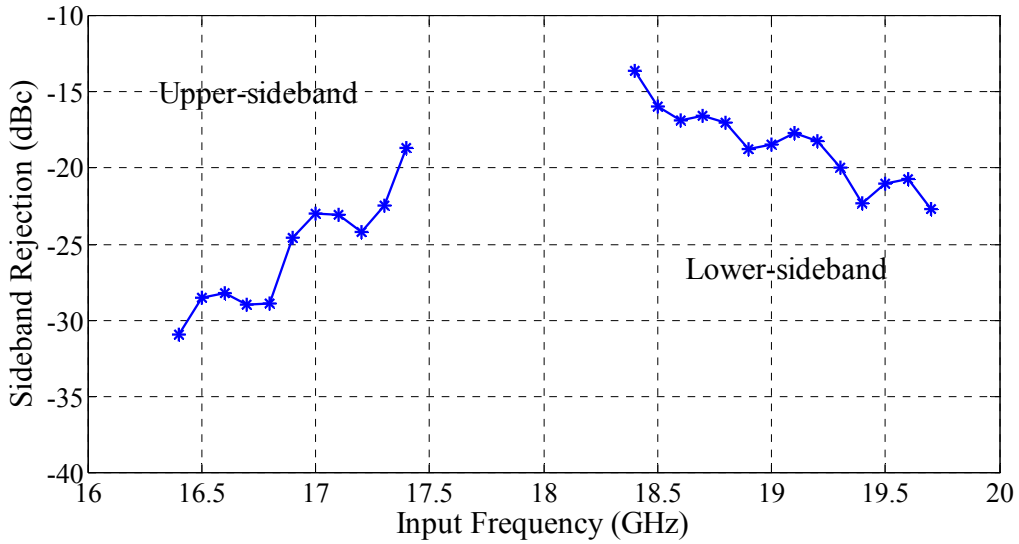


Fig. 4.72 Measured image rejection vs. input frequency

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Chapter 5 HIGH-SPEED CURRENT STEERING DAC

5.1 Introduction

Recently developed high-speed wireless communication systems have motivated system-on-chip solutions with RF, analog and even digital circuits being integrated on a single chip. Aiming at fully-integration of our UWB transceiver, high-speed IQ-channel DACs become an impending need. As specified in Chapter 2, the DAC is expected to reach a fast sampling clock frequency up to 1 GHz while maintaining 6-bit resolution.

Of several technology and architecture alternatives, CMOS current-steering DAC architectures are particularly suitable for UWB application for the following reasons [1]: 1) they can be designed in a standard CMOS technology, with evident cost and power consumption advantages in the integration with other building blocks, and 2) they are intrinsically faster and more linear than competing architectures such as resistor-string DAC's. Therefore, it becomes the preferred choice in our design.

5.2 Current-steering Topologies

Current-steering DACs are based on an array of matched current sources that are switched to the output [2]. There different topologies are possible depending on the implementation of this current array, namely the binary-weighted, the thermometer-coded, and the segmented architecture.

- Binary-weighted architecture

In the binary-weighted implementation, every switch switches a current to the output that is twice as large as the next least significant bit (LSB). The digital input code directly controls these switches. The advantages of this architecture are its simplicity and the small required silicon area, as no decoding logic is required. There are several major drawbacks, however, which are all associated with major bit transitions [3]. Taking 6 bits DAC as example, at the mid-code transition (0 1 1 1 1 1 to 1 0 0 0 0 0), the most significant bit (MSB) current source needs to be matched to the sum of all the other current sources to within 0.5 LSB's. This is difficult to achieve. Because of statistical spread, such matching can never be guaranteed. In addition, the errors caused by the dynamic behavior of the switches, such as charge-injection and clock feed-through, result in glitches in the output signal. This problem is most severe at the mid-code transition, since all switches are switching simultaneously. Such a mid-code glitch contains highly nonlinear signal components, even for small output signals and will manifest itself as spurs in the frequency domain.

- Thermometer-coded architecture

In contrast to binary-weighted topology, every unit current source is addressed separately in thermometer-coded architecture. For instance, there are 2^6=64 unit current sources for 6-bit DACs. The digital input code is then converted to a thermometer code that controls the switches. When the digital input increases by one LSB, one more current source is switched from the negative to positive side.

Assuming positive-only current sources, the analog output is always increasing as the digital input increases. Hence, the DAC has a guaranteed monotone behavior using thermometer-coded architecture.

Furthermore, there are several other advantages for a thermometer-coded DAC compared to its binary-weighted counterpart. Firstly, the matching requirement is much relaxed: 50% matching of the unit current sources is good enough for the differential nonlinearity (DNL) better than 0.5 LSB. Even at the mid-code, a 1 LSB transition from 0 1 1 1 1 1 to 1 0 0 0 0 0, only one current source is switched as the digital input only increases by one. This greatly reduces the glitch problem. On the other hand, the magnitude of a glitch is proportional to the number of switches that are actually switching. So for a small step, the glitch is small, and for a large step, the glitch is large. Since the number of switches that switch are proportional to the signal step between two consecutive clock cycles, the magnitude of the glitch is directly proportional to the amplitude of the signal step. Therefore, theoretically it will not cause any nonlinearity in the DAC output signal.

Nevertheless, one major drawback of the thermometer-coded DAC is the fact that the area used by the decoding and interconnections inside the matrix increases, and consequently the process and electric systematic errors become more difficult to compensate. Another direct consequence is often a reduction in the maximum operating speed.

- Segmented architecture

To leverage the performance, complexity and chip area, most of the

current-steering DACs are implemented using a segmented architecture [1]-[3]. In this case, the DAC is divided into two sub-DACs: the M most significant bits are implemented using thermometer architecture while the N-M least significant bits are implemented in a binary way. An extension to the segmented structure is to use multi-segmentation. For example, the M MSBs are thermometer coded in one cluster, the K LSBs are kept binary weighted, and the N-M-K intermediate bits are also thermometer coded in another separate cluster.

5.3 System Design and Consideration

To achieve good static and dynamic specifications with a reasonable decoder power, area, and complexity, a current steering segmented 5+1 architecture is adopted for our 6-bit 1G/s DAC. First, the 5 MSB's are linearly decoded; then, the last LSB is binary weighted. Fig. 5.1 presents the block diagram of the DAC architecture.

The key point to preserving a very high update rate is to keep an intrinsically simple and compact decoding logic. Hence, a two-stage row-column decoding logic is implemented for the 5 MSBs, which only require NAND and NOR gates with three or two inputs. Moreover, two-dimensional centroid switching sequence, similar to the one described in [1], is implemented. By simultaneously selecting a symmetrically located current source in each of the four quadrants of the matrix, the systematic error is minimized. More descriptions on the thermometer decoder will be given in the later sections.

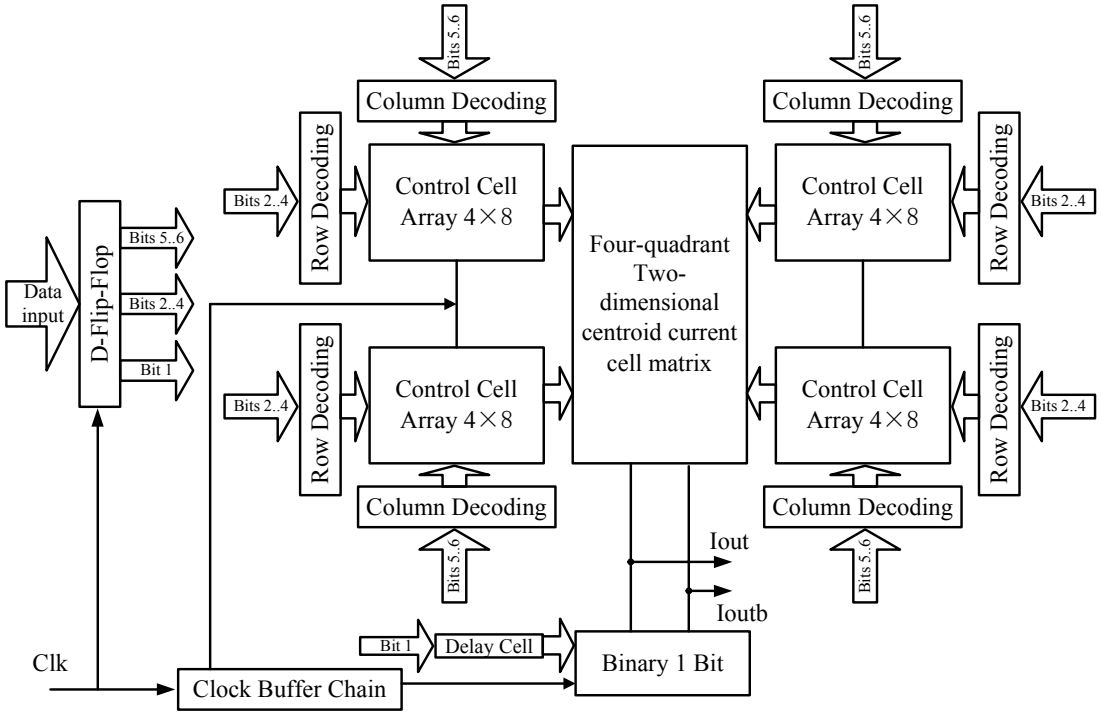

Fig. 5.1 Block diagram of the proposed DAC architecture

In addition, as shown in Fig. 5.1, the parallel input data are first captured and synchronized by the D-Flip-Flop before they are processed by the decoding logic. The current sources switching between MSBs and LSB are synchronized by clock and data delay cells inserted before 1st binary bit. Furthermore, additional synchronization of the control signals of the switching transistors for all input codes is achieved by using one static latch per current cell before the switching transistors.

5.4 Implementation of Current Source

The task of the current source is to accurately generate the required currents, to properly switch these currents to the differential output nodes, and finally to convert the current linearly into a voltage on the output node. Inaccuracies on the sources in a current cell matrix, however, can be caused by random variations and by systematic

influences, such that the matching of the current sources becomes critical.

- Random Mismatches

Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices. The random error of the current sources is determined by matching properties, which determine the dimensions of the unit current source. A widely accepted model for random mismatch is a normal distribution with zero mean and a variance dependent on the gate-with W and the gate-length L of the devices [4]. The deviations of threshold voltage and trans-conductance are expressed as Equations (5.1) and (5.2).

$$\delta(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \tag{5.1}$$

$$\delta(\frac{\Delta\beta}{\beta}) = \frac{A_\beta}{\sqrt{WL}} \tag{5.2}$$

where A_{VT} and A_β are mismatch technology constants. E.g. for TSMC 0.18 process, A_{VT} is about 3 ~ 4 mv*μm, and A_β is about 0.8 ~ 1 % μm [5].

It is well known that, the drain output current of a CMOS transistor at saturation region can be calculated from

$$I_D = \frac{1}{2}\beta(V_{GS} - V_T)^2 \tag{5.3}$$

where $(V_{GS}-V_T)$ is the gate overdrive voltage of the current source.

Note that

$$\Delta I = \frac{\partial I}{\partial \beta}\Delta\beta + \frac{\partial I}{\partial V_T}\Delta V_T \tag{5.4}$$

From Eqs. (5.3) and (5.4) we can derive

$$\frac{\Delta I}{I} = \frac{\Delta \beta}{\beta} - 2\frac{\Delta V_T}{(V_{GS} - V_T)} \tag{5.5}$$

Thus, we have

$$\left(\frac{\Delta I}{I}\right)^2 = \left[\delta\left(\frac{\Delta \beta}{\beta}\right)\right]^2 + \frac{4}{(V_{GS} - V_T)^2}\left[\delta(\Delta V_T)\right]^2 \tag{5.6}$$

From Eqs. (5.1), (5.2) and (5.6), the minimum required gate area (WL) of the unit current source transistor is derived as

$$WL = \left[A_\beta{}^2 + \frac{4A_{VT}{}^2}{(V_{GS} - V_T)^2}\right] \Big/ \left(\frac{\delta I}{I}\right)^2 \tag{5.7}$$

As explained by Eq. (5.7), the minimum required area can be decreased by increasing the overdrive voltage (V_{GS}-V_T).

On the other hand, assuming a normal distribution for the unit current sources, the required relative standard deviation of a unit current source can be estimated from statistical yield model [6], which is given by

$$\frac{\delta(I)}{I} \le \frac{1}{2C\sqrt{2^N}} \tag{5.8}$$

where N denotes the resolution of the DAC, and the parameter C is found from the inverse function of the normal cumulative function:

$$C = inv\_norm\left(0.75 + \frac{INL\_yield}{4}\right) \tag{5.9}$$

The INL_yield is defined as the ratio of the number of DAC with an INL smaller than 1/2LSB to the total number of tested DAC.

For example, if we want to achieve INL with a yield of larger than 99.2 % for a 6 bit DAC, from the above equations, we need $\frac{\delta(I)}{I} < 2.17\%$.

- Systematic Errors

Systematic mismatch can be subdivided into linear gradient mismatch and parabolic gradient mismatch. The linear gradient mismatch is mainly due to the well-known radial pattern of the oxide thickness over the wafer, whereas parabolic gradient mismatch is normally caused by temperature gradients and stress gradients. These systematic error sources are two dimensional (2-D) in nature. To compensate 2-D systematic errors in thermometer-coded architecture, one must switch the current sources with a centroid sequence. Therefore, the well known two-dimensional centroid switching sequence is applied, which is explained in Fig. 5.2. The unit current sources in the matrix are switched on or off following the number from 1 to 31 indicated in Fig. 5.2.

27	25	26	28		28	26	25	27
19	17	18	20		20	18	17	19
11	9	10	12		12	10	9	11
3	1	2	4		4	2	1	3
7	5	6	8		8	6	5	7
15	13	14	16		16	14	13	15
23	21	22	24		24	22	21	23
31	29	30				30	29	31
31	29	30				30	29	31
23	21	22	24		24	22	21	23
15	13	14	16		16	14	13	15
7	5	6	8		8	6	5	7
3	1	2	4		4	2	1	3
11	9	10	12		12	10	9	11
19	17	18	20		20	18	17	19
27	25	26	28		28	26	25	27

Fig. 5.2 Two-dimensional centroid switching sequence

- Cascode current cell

The impedance at the output node is determined by a parallel circuit of the output resistor and a variable number of unity current cells. As is generally known, the finite output resistance of any non-ideal current source in the DAC will strongly influence both the static and the dynamic performance [7]. Therefore, cascode current source is designed, which is shown in Fig. 5.3. On the other hand, the cascode configuration can isolate the output nodes of the current sources (M1) from output voltage fluctuations, and hence provides more constant voltage at drain output as well as the better matched unit current.

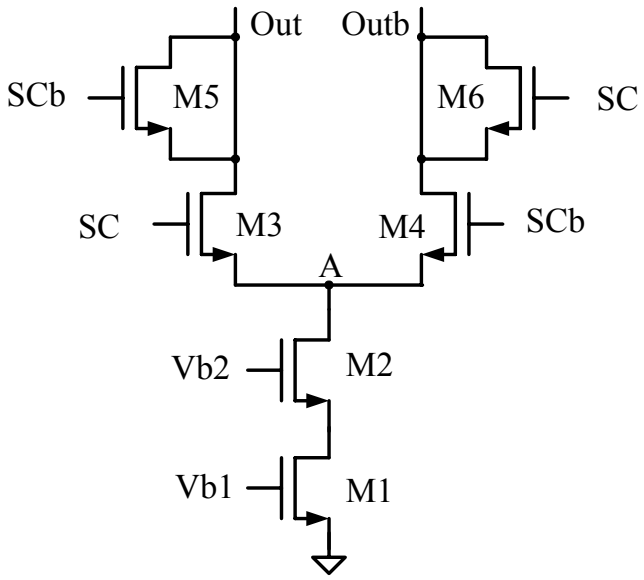

Fig. 5.3 Schematic of the current cell

- Feed-through and Charge Injection

The coupling of the switching control signals to the output lines through the parasitic gate-drain capacitance of the switching transistors is one of the main contributions to the glitch. Several solutions have been proposal to minimize this error source. One of the solutions is to isolate the drain of the switching transistors

from the output lines by adding another cascoded transistor. In our work, alternately, the signal feed-through and charge injection are compensated by connecting in parallel dummy transistors driven by the complementary control signals, as shown in Fig. 5.3. The dummy transistors M5-6 are designed to have half size of the switching transistors M3-4 for well matching.

5.5 Implementation of Latch

In addition to the charge-injection and feed-through which have been addressed, the dynamic performance of the DAC can be characterized by other nonlinearities associated with current source switching. These nonlinearities are mainly caused by the following effects:

1). an imperfect synchronization of the input signals of the current switches;

2). and current variation due to a drain voltage variation of the current sources caused by the fact that both current switches are simultaneously in the off-state.

To synchronize all the control signals, one static latch per current cell is directly placed in front of the switching transistors (see M3-M4 in Fig. 5.3). As depicted in Fig. 5.4, the latch is controlled by one global clock signal. It provides the two complementary signals needed at the input of the current switches.

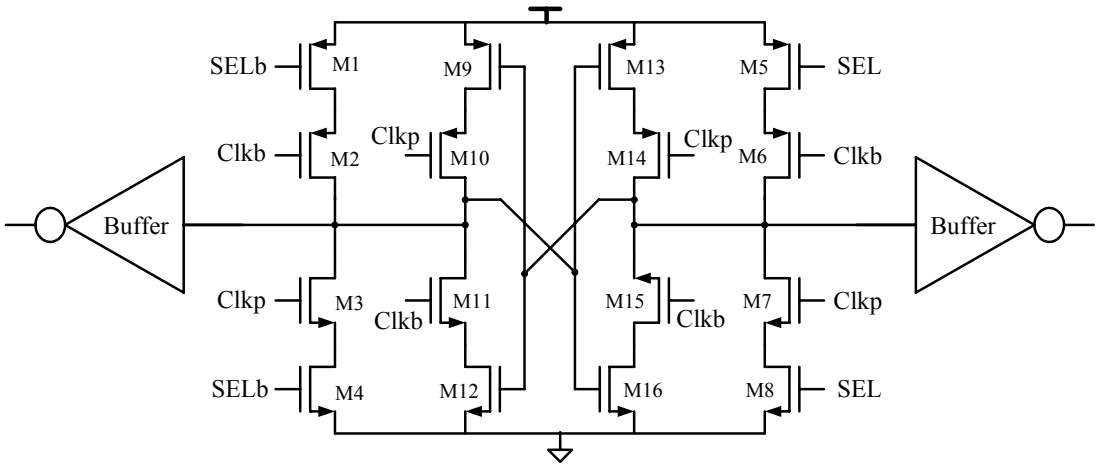

Fig. 5.4 Schematic of the proposed latch

To address the voltage fluctuation problem, conventionally, the latch also is designed to shift the crossing point of the switching control signals, so that as soon as one of the switching transistors begins to switch off, the complementary switching transistor starts to switch on. However, another problem comes out if the crossing point of the control signals is apart from the middle point. Because of the asymmetry of the control signals, the feedthrough of the control signals to the output nodes through the gate-source capacitance of the switching transistors can not be cancelled. This inevitably increases the glitches at output. Moreover, it becomes more difficult to implement the dummy transistors since more complementary control signals are required. As a compromise, in our work, the crossing point of the control signals is clipped at middle.

As illustrated in Fig. 5.4, the combination of the PMOS and NMOS transistors results in the crossing point that is easier to control. Furthermore, the positive feedback loop formed by M9~M12 with extra complementary clock-controlled transistors is included, which not only reduces the switching time but also helps to

suppress the glitch introduced by the clock.

5.6 The Thermometer Decoder

As mentioned previously, a two-stage row-column decoding logic is implemented for the 5 MSBs with thermometer code. Fig. 5.5 presents the block diagram of the thermometer decoder. The 3 most significant bits B6~B4 are decoded into 7 bits thermometer code from R7 to R1, which is used to control the unit current cell matrix in row. Besides, the two intermediate bits, B3 and B2, are decoded into 3 bits thermometer codes from C3 to C1, which is then applied to select the unit current cell matrix in column.

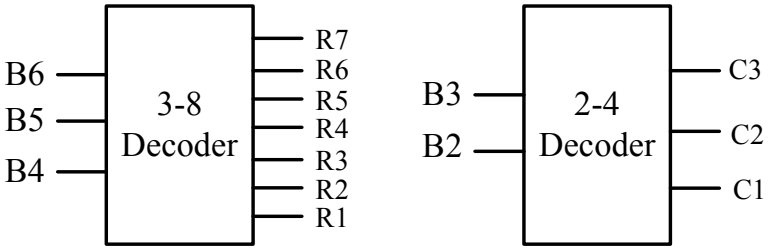

Fig. 5.5 Block diagram of the thermometer decoder

The unit current sources in the current cell matrix are selected by a control matrix using the row and column outputs from the thermometer decoder. The select signals determine if a specific current source should be turned on or off. The block diagram of the thermometer control matrix is explained in Fig. 5.6. In each current control cell, three control signals, one column and two row signals are used for logic operation. The control output is given by

$$SEL = R_n \left(R_{n+1} + C_n \right) \tag{5.10}$$

where n=0…8 for row control R, and n=1…4 for column control C. Equation (5.10)

can be realized by a simple 3-input gate logic.

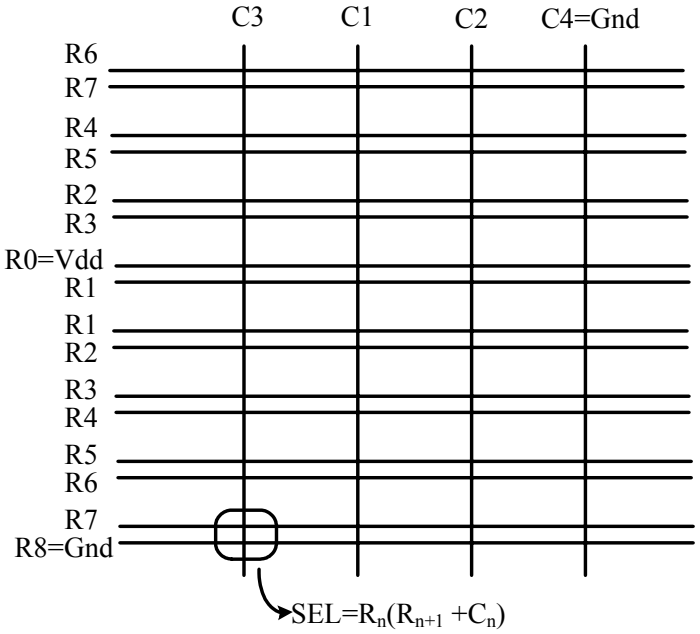

Fig. 5.6 Block diagram of the thermometer control matrix

5.7 Layout Design and Considerations

In order to reduce the current cell matrix area to achieve the best matching results, all the decoding logic and the associated interconnections are moved to outside of the current cell matrix. Specifically, the latches together with switching transistors (M3-M4) and the cascode transistors (M2) are placed in a separate region from the current source transistors (M1). As illustrated in Fig. 5.7, the current source matrix is located in the center of the layout; inside the matrix all transistors are perfectly identical to minimize the transistor mismatches. To avoid edge effects, two dummy rows and columns have been added to surround the current source transistors array. Furthermore, all the current cell transistors are built in deep N-Well to minimize the noise coupling from the substrate, which is available in TSMC 0.18-μm

CMOS process.

In addition, to minimize the systematic error introduced by the voltage drop in the analog ground lines of the current source transistors, sufficiently wide Metal 6 have been used. These are drawn on top of the transistors. The clock lines and the output lines are planned carefully to minimize the coupling between the digital signals and the analog output signals. The digital coupling through the substrate is reduced by the intensive use of substrate contacts and guard rings.

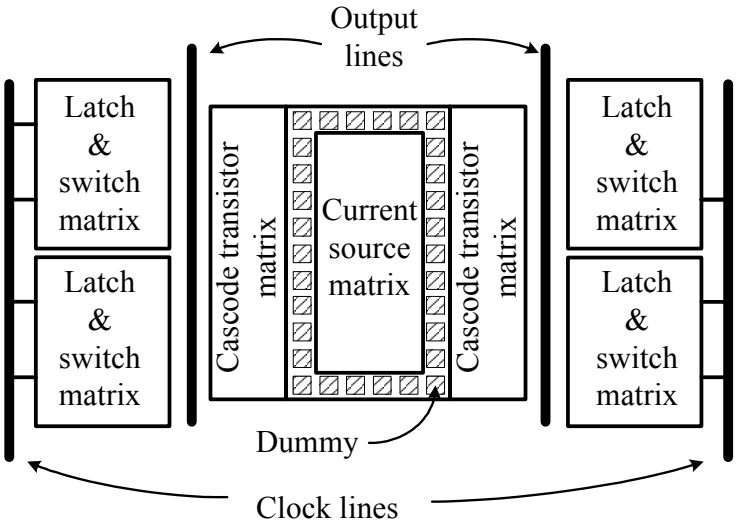

Fig. 5.7 Layout floor-plan of the DAC

Moreover, the clock lines are distributed by several stages with a tree-structure network to ensure that all the clock signals have the same delay. Hundreds of pico-farad on-chip decoupling capacitance (by MOS cap) have been used to decouple the power supply lines, which help to reduce the effects of the parasitic bondwire and metal line inductance.

5.8 Measurement Results

The proposed 6-bit current steering DAC for the UWB transceiver is designed

and fabricated in TSMC 0.18-μm CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers. Fig. 5.8 shows the die photograph of the two DACs for IQ channels, which occupies a core area of 1.6×0.95 mm^2.

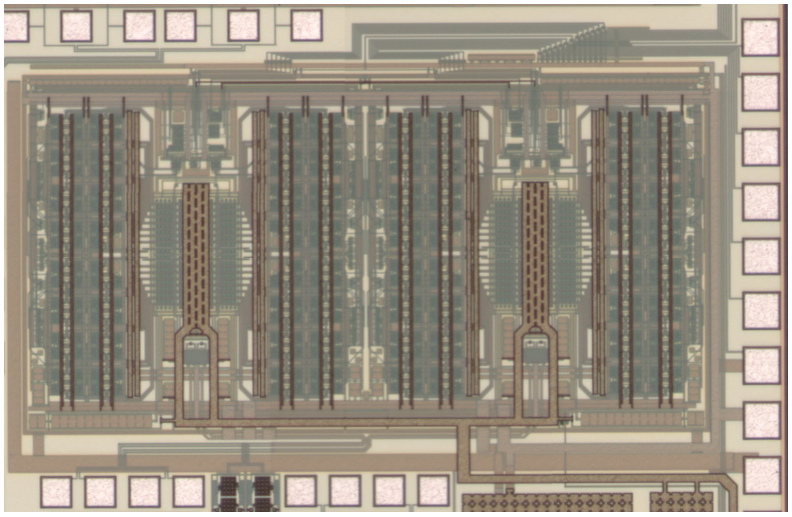

Fig. 5.8 Die photo of the IQ DACs

HP 80000 data generator is used to measure the proposed DAC, which is able to deliver six data channels and two complementary clock channels with a fastest clock frequency of 1 GHz. In addition, the required 6-bit data patterns with 8192 bits in length are downloaded into HP 80000 through a Labview program. Nevertheless, the maximum reliable pattern frequency from HP 80000 is actually limited to around 900 MHz. As such, the maximum sampling frequency in our measurement is limited to 900 MHz as well. Operated under 1.8-V supply voltage, the IQ-channel DACs consume a total current of 45 mA at 900MHz sampling.

To measure the dynamic performance of the DAC, an on-chip open-drain buffer with SGS pads is included at output for testing purpose. The output signals taken from open-drain buffer with on-wafer SGS probing are then connected to Agilent E4440A spectrum analyzer. A worst-case SFDR of 33 dB with input frequency up to

250 MHz is measured. Fig. 5.9 and Fig. 5.10 show the output spectrums of the DAC at 3.5 MHz and 228.5 MHz inputs with 900 MHz sampling.

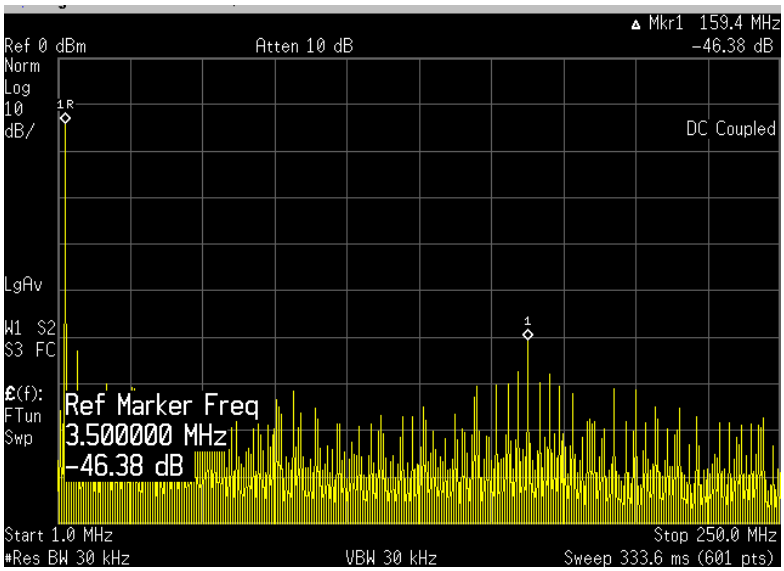

Fig. 5.9 Output spectrum of the DAC at 3.5 MHz input with 900 MHz sampling clock frequency

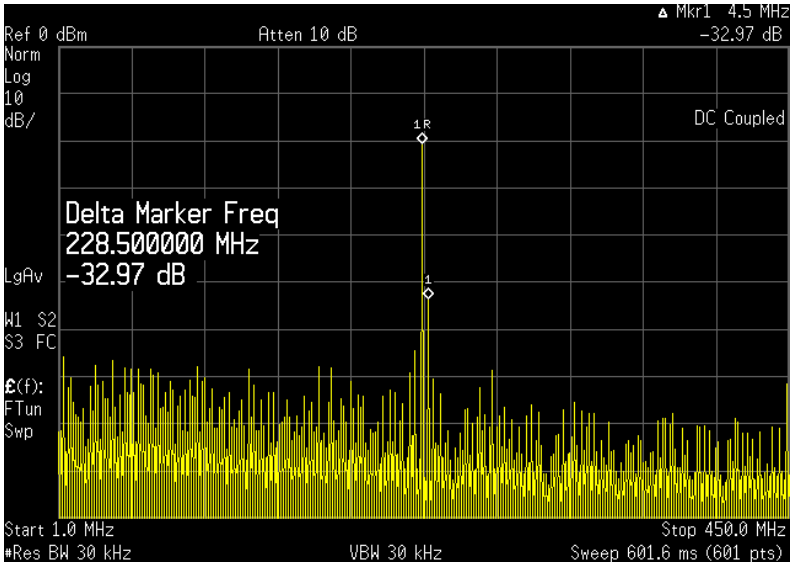

Fig. 5.10 Output spectrum of the DAC at 228.5 MHz input with 900 MHz sampling clock frequency

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Chapter 6 INTRODUCTION TO THE OTHER BUILDING BLOCKS

6.1 Wideband Low Noise Amplifier

6.1.1 Design of the Wideband LNA

To comply with the proposed 9-band UWB transceiver, a wideband LNA operating from 3GHz to 8GHz is required [1]. The LNA must feature wideband input matching to an impedance of 50-Ω for maximum power transfer and for out-of-band interferer filtering. Moreover, it must have a relatively flat gain over the entire bandwidth, minimum possible noise figure (NF), and low power consumption. To suppress the noise contribution from the latter stages, the LNA gain is required to be larger than 22dB, which imposes a great challenge of an extremely large gain-bandwidth product (GBW).

Due to high-frequency and wideband operation, the maximum gain of a single-stage amplifier is very limited. As a consequence, a 3-stage LNA is proposed as shown in Fig. 6.1 to deliver a maximum gain of 22dB over such a wide bandwidth. In addition, variable gain of more than 12 dB is implemented at the 3rd stage by current steering to accommodate low gain requirement and thus to relax the linearity requirement for large input signals.

Wideband input impedance matching network can be either lossless or lossy. For a lossless matching, the matching network is composed of reactive components, and energy is ideally conserved. As a result, there would exist a limit on the

maximum bandwidth over which an arbitrarily good impedance matching can be obtained [2]. This kind of matching is proposed in [3] with multiple LC sections to simultaneously achieve wideband matching, low NF, and low power consumption. However, source-degeneration inductors need to be employed, which would lead to gain degradation and rapid NF increase at high frequencies. Moreover, many on-chip inductors in the matching network would occupy very large chip area.

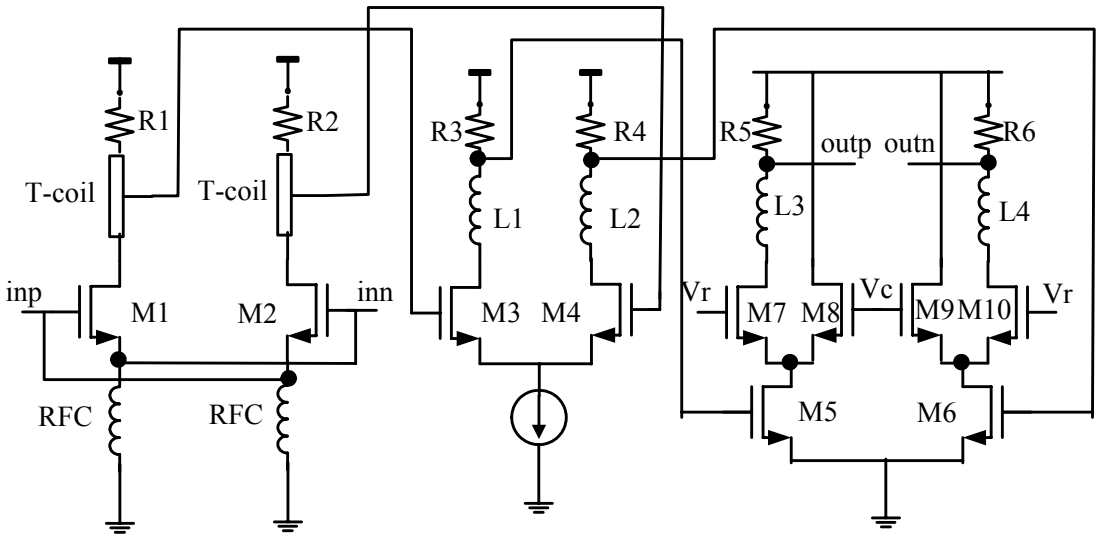


Fig. 6.1 Schematic of the proposed 3-stage wideband LNA with variable gain

On the other hand, for lossy matching, due to their resistive components, the energy in the matching network is not conserved, and there is no limit for the good wideband matching. The matching network can be much simpler, at the same time, better and more robust matching over process variation can be achieved.

To eliminate source-degeneration inductors, a common-gate lossy matching input stage is adopted. The input differential pair is cross-coupled [4]. The effective transconductance becomes 2*gm, where gm is the transconductance of M1 (M2). For 50-Ω matching requirement, the power consumption is reduced by half, and the noise factor F of the first stage is reduced from 1+ϒ to 1+ϒ/2, where ϒ represents the

channel thermal noise coefficient.

To enable the LNA to operate with a wide bandwidth, T-coil and series inductive peaking are used as output loadings. Fig. 6.2 shows the schematic of the T-coil. If the load capacitor C_L is much larger than the parasitic capacitor at the T-coil's input port, with the conditions of k=1/3, $L_1=L_2=3*R^2C_L/8$, $C_b= C_L/8$, the T-coil is capable of almost tripling the bandwidth [5].

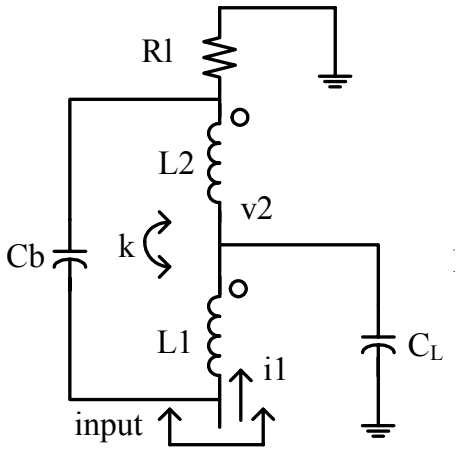


Fig. 6.2 Schematic of the T-coil network

Compared with the T-coil, the series-peaking networks are simpler, easier to be modeled, occupy less area, and actually achieve larger bandwidth extension when the two capacitors at the two ports are comparable. However, they will suffer from some peaking at high frequencies. Because the first-stage LNA's transistor size is half of those in the last two stages, the parasitic capacitance at its drain node is relatively small. In addition, the gain flatness is important in order to suppress the noise contribution of the latter stages over the whole band. As a consequence, the first LNA stage uses a T-coil as its load while the last two stages use inductive series peaking instead.

6.1.2 Measurement Results of the LNA

Operated under 1.8-V supply, the proposed 3-stage LNA dissipates a total current of 15.5mA. As plotted in Fig. 6.3, the LNA measures the S11 of better than -13 dB within the whole 9 frequency bands from 3.1 GHz to 8.0 GHz.

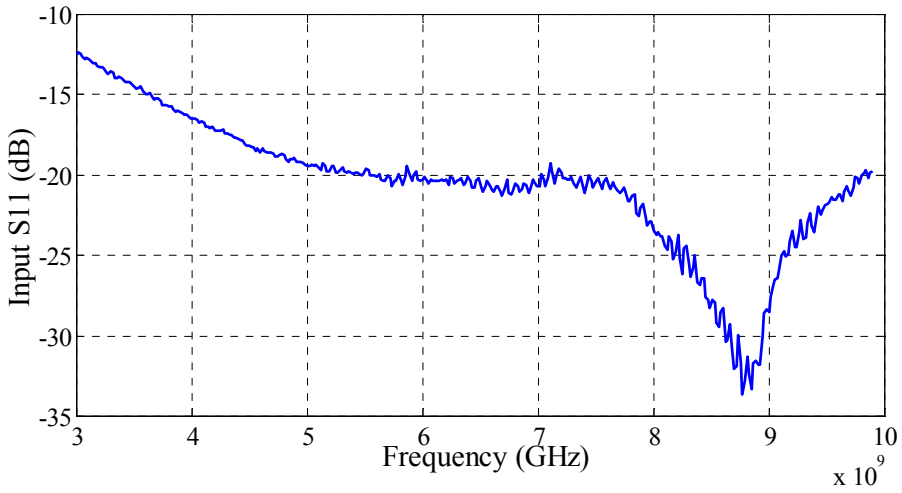


Fig. 6.3 Measured S11 of the proposed LNA

Fig. 6.4 plots the measured voltage gain versus input frequency. The LNA achieves the maximum voltage gain of larger than 22.4 dB, which is necessary to suppress the noise contributions from the latter stages.

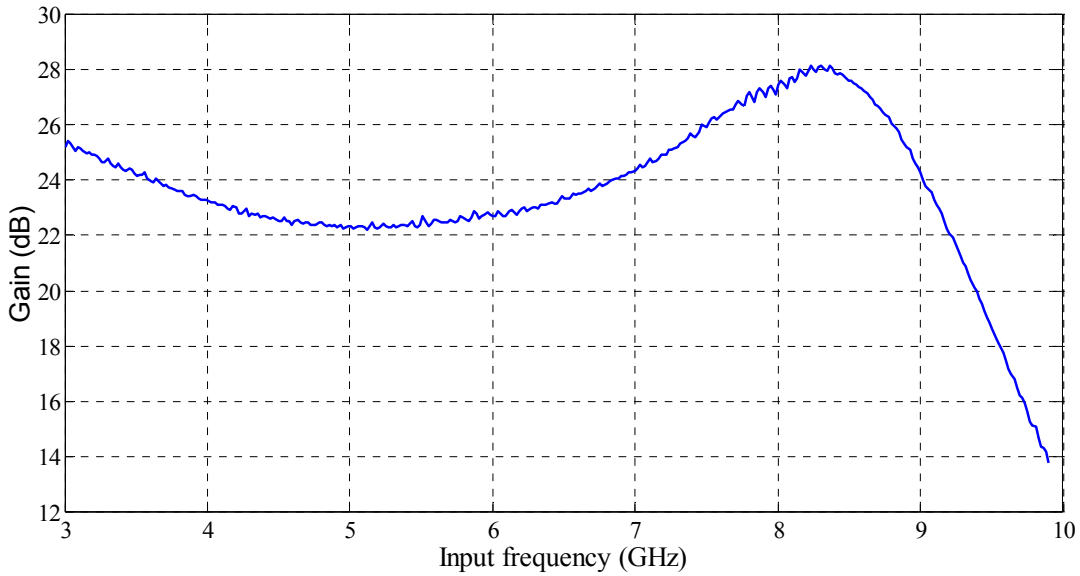


Fig. 6.4 Measured voltage gain of the LNA

The measured NF of the LNA is illustrated in Fig. 6.5, which varies from 6.3 dB to a minimum value of 5 dB as the input frequency increases. From simulation, the NF of the LNA varies from 5.3 dB to 4.1 dB as the frequency increases from 3.1 to 8.0 GHz. Hence, the measured LNA's NF of 1.3 dB worse at lowest band is expected. There are several potential reasons: Firstly, the RF choke inductors in the first stage have relatively smaller impedance at low frequency bands than that at the high frequency bands, which make the S11 7 dB worse as plotted in Fig. 6.3; Secondly, as shown in Fig. 6.4, the overall gain of the LNA at high frequency bands is higher than the low bands. More detailed explanations on the NF of the LNA can be found in Reference [12] (Section 4.3.1.D, Pages 100-104). Table 6.1 summarizes the measured performances of the wideband LNA.

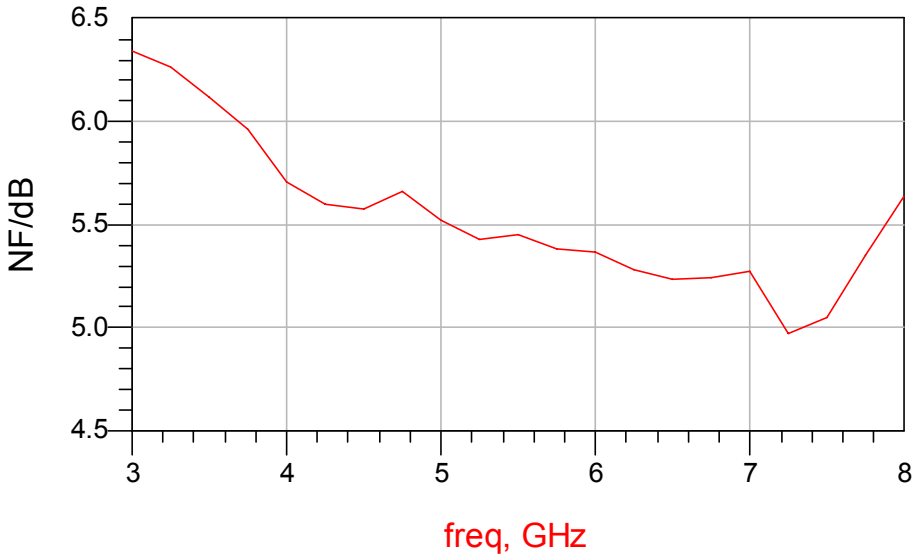


Fig. 6.5 Measured NF plot of the LNA

Table 6.1 Performance summary of the proposed LNA

Voltage gain (dB)	S11 (dB)	Noise figure (dB)	IIP3 (dBm)	Power consumption (mA)
> 22.4	< -13	5 ~ 6.3	-6	15.5

6.2 Mixers

6.2.1 Combined High-Frequency Up-Down Mixer

In our proposed UWB transceiver, two-stage mixers are required to perform dual conversion with the first IF1 at 2.9 GHz and the second IF2 at DC. A combined mixer is proposed for both RF-IF1 down-conversion in the RX and for the IF1-RF up-conversion in the TX, and its schematic is shown in Fig. 6.6. Unlike in the conventional Gilbert-type mixer, the LO switches of the combined mixer are moved to the bottom of the transconductors so that they can be shared between the RX and TX. With such a combined mixer configuration, the capacitive loading to the synthesizer's LO1 output is reduced by half. In addition, the LO1 input devices can be laid out very close to the synthesizer output, which minimizes the interconnection between the synthesizer and the mixer so as to further reduce the loading and to avoid a need of power-hungry on-chip buffers.

The transconductors and the loads are switched by the controlling signals EN and ENB to enable down-conversion or up-conversion for RX-mode or TX-mode operation one at a time, respectively. On the other hand, in this mixer topology, large voltage swings at source nodes of the gm transistors (Nodes A & B) are required to completely switch the transconductors. Consequently, series peaking inductors L3 and L4 are inserted to extend the bandwidth to maximize the voltage swing at Nodes A and B. For the IF1-RF TX-mixer, T-coil is selected as the load to achieve wideband output. Further, an output buffer with 50-Ω load is added at the output to obtain output impedance matching for direct connection to the off-chip pre-selection filter

without a need of a power amplifier. Since the IF1 frequency is fixed at 2.9 GHz, LC tanks with Q of around 5 are employed as the loads for both the RF-to-IF1 RX-mixer and the BB-to-IF1 TX-mixer. Wherein, the LC tanks also work as a band-pass filter to provide additional narrow-band filtering.

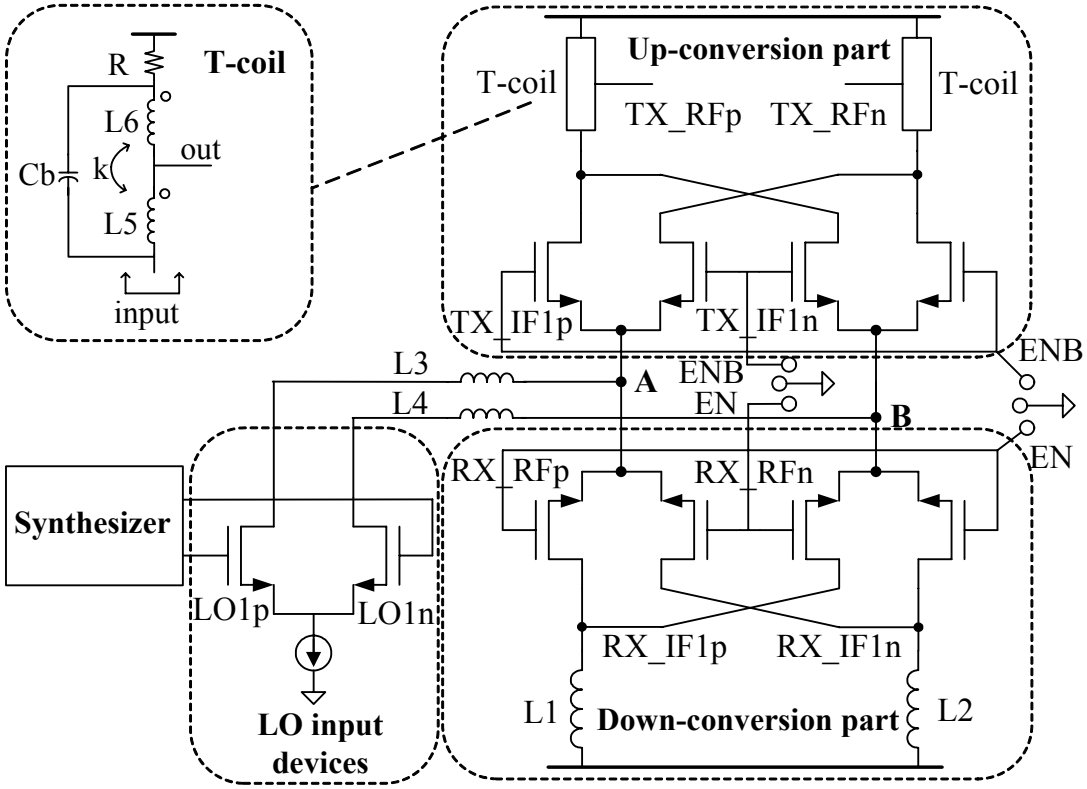


Fig. 6.6 Schematic of the proposed combined mixer for both RF down-conversion in RX and up-conversion in TX

6.2.2 IQ Mixers

The second-stage receiver IQ mixers employ the conventional Gilbert cell for a fixed and lower frequency IQ LOs at 2.9GHz. Resistive load is employed since the baseband output frequency only covers the range from 2MHz to 264MHz. Moreover, inductive degeneration is adopted to improve its linearity, which is shown in Fig. 6.7.

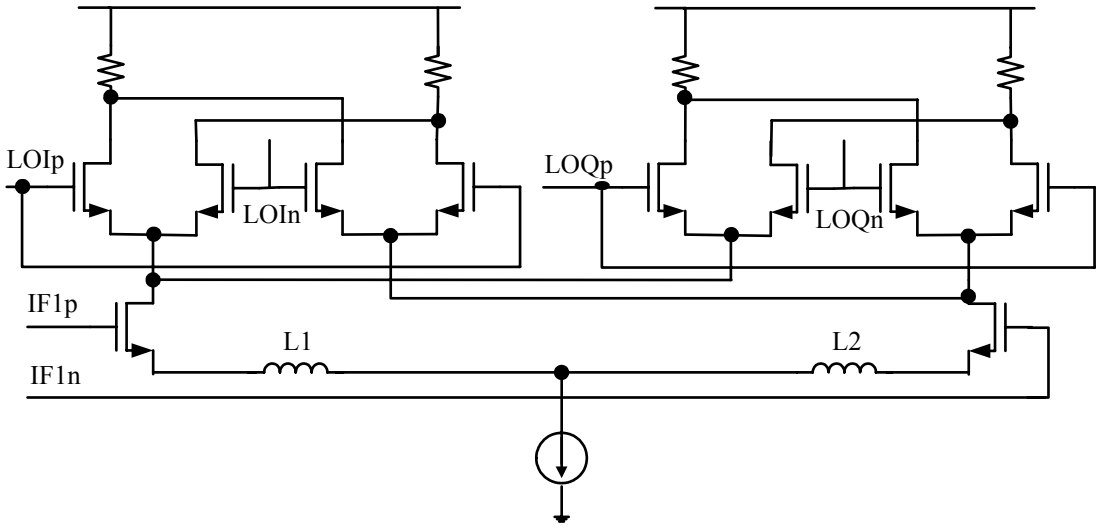


Fig. 6.7 Schematic of the receiver IQ mixers

In contrast, the transmitter BB-IF1 mixer contains both IQ baseband inputs and IQ LO signals. The output currents from two identical mixers are then combined to achieve single-sideband output. In addition, no degeneration is implemented in the BB-IF1 up-convention mixer.

6.2.3 Measurement Results of the Mixers

The two-stage mixers in the receiver draw a total current of 7.5 mA from 1.8-V supply. Table 6.2 shows the summary of the combined performance of the two stages down-conversion mixers. The up-conversion mixers' performances together with the transmitter performances will be addressed in the next chapter.

Table 6.2 Summary of the two-stage down-conversion mixers performances

Voltage gain (dB)		Noise figure (dB)	IIP3 (dBm)		Power consumption (mA)
Mixer1	Mixer2		Mixer1	Mixer2	
1.1	5.6	~21.6	~10	~6.5	7.5

6.3 Receiver-filter

6.3.1 Design of the Receiver Channel Selection Filter

In addition to the preliminary channel-selection provided by the LC-tank in the 1st-stage mixer, a third-order Elliptic ladder low-pass channel-selection filter (CSF) is employed for both IQ channels in the receiver chain to provide additional adjacent-channel attenuation. The filter is based on Gm-C architecture and should have a -3dB bandwidth of around 260 MHz and a fixed gain of about 5 dB. Fig. 6.8 shows the topology of the designed receiver CSF, in which identical transconductance cells are used for better matching. Furthermore, to reach the required high frequency input while minimizing the power consumption, the parasitic capacitance is taken into account to constitute the integration capacitance together with additional MIM capacitors. To trade off the gain, the noise and the linearity performance simultaneously, gain stages are applied both in the front of and at the end of the filter.

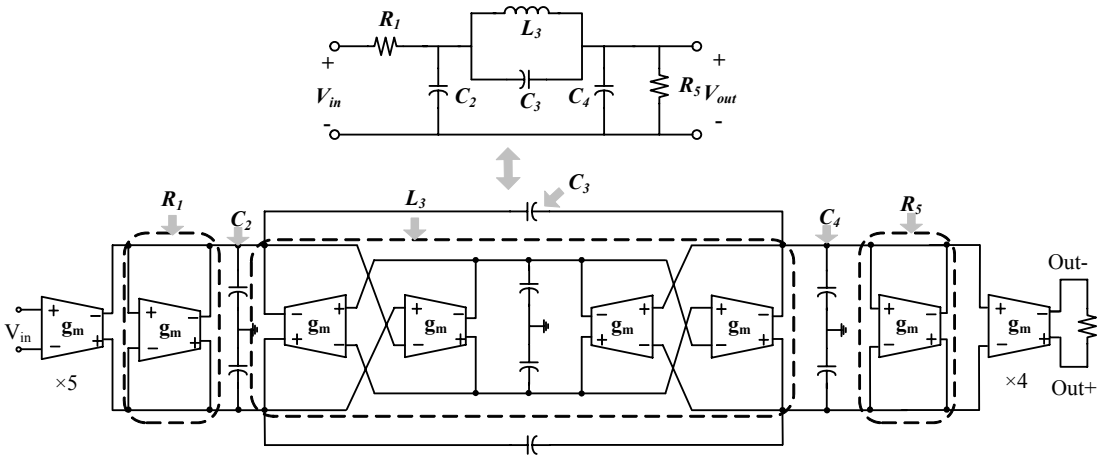


Fig. 6.8 Schematic of the receiver channel-selection-filter

The schematic of transconductance cell is shown in Fig. 6.9. To minimize the internal nodes capacitance of the transconductance cell to achieve high frequency

operation, a simple transconductance topology with negative-G_m cell and diode-connected PMOS is utilized as load. This not only helps to improve the output impedance but also can fix the output DC bias point by the loading itself.

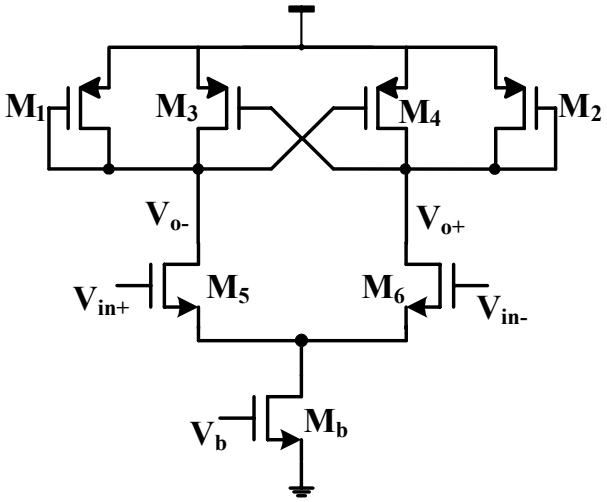


Fig. 6.9 Schematic of the Gm-cell in the CSF

6.3.2 Measurement Results of the Receiver Filter

Operated under a 1.8-V supply, both I- and Q-channel CSFs draw a total current of 44 mA. Fig. 6.10 shows the measured AC response of the receiver CSF with a -3 dB bandwidth of 253 MHz and the adjacent-channel attenuation of 20.1 dB at 528 MHz offset. Whereas, these results have not included the source resistance effect from the previous mixer stage.

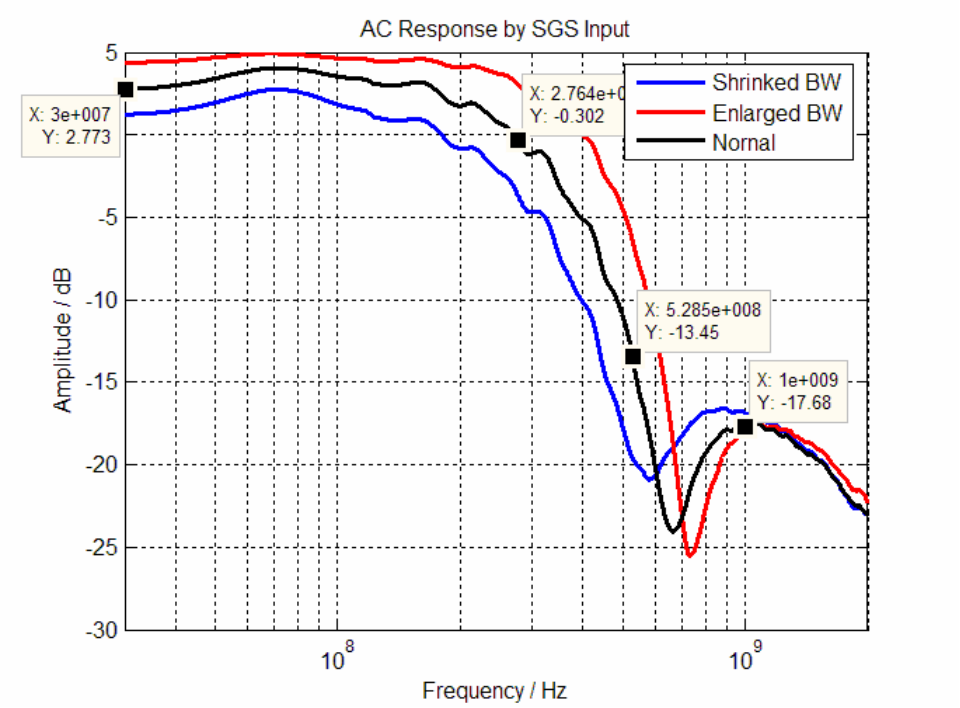


Fig. 6.10 Measured AC response of the CSF

As plotted in Fig. 6.11, the filter achieves an output P-1dB of -2.7 dBm. In addition, a NF of better than 13 dB is measured for the input frequency range from 1MHz to 260MHz. Table 6.3 shows the summary of the measured performances.

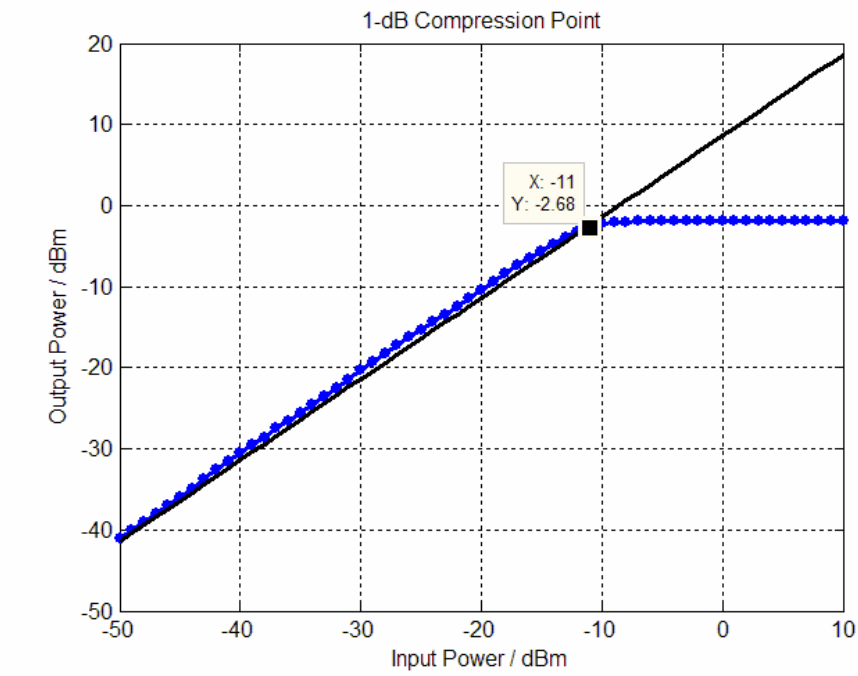


Fig. 6.11 Measured output P-1dB plot of the CSF

Table 6.3 Summary of the receiver CSF

Attenuation (dB)	-3 dB bandwidth	Noise figure (dB)	OP-1dB (dBm)	Power consumption (mA)
> 20 dB @ 528 MHz	253 MHz	< 13 dB	-2.7 dBm	44 mA

6.4 Variable Gain Amplifier

6.4.1 Design of the VGA

To cover the full dynamic range of the input signals to the UWB receiver, a 3-stage VGA with variable gain range from 10 to 50 dB is designed. As shown in Fig. 6.12, the overall variable gain is distributed over the first two stages, each with a variable gain from -4 dB to 17 dB. In addition, linear-in-dB exponential control circuit is included to provide an exponential gain characteristic, which is desired for the receiver to maintain a constant settling time with different input amplitudes in the automatic gain control (AGC) loop. In contrast, the last stage has a constant gain of 17 dB for better linearity, which is followed by a source follower as an interface buffer to drive the large input capacitors of the ADC stage.

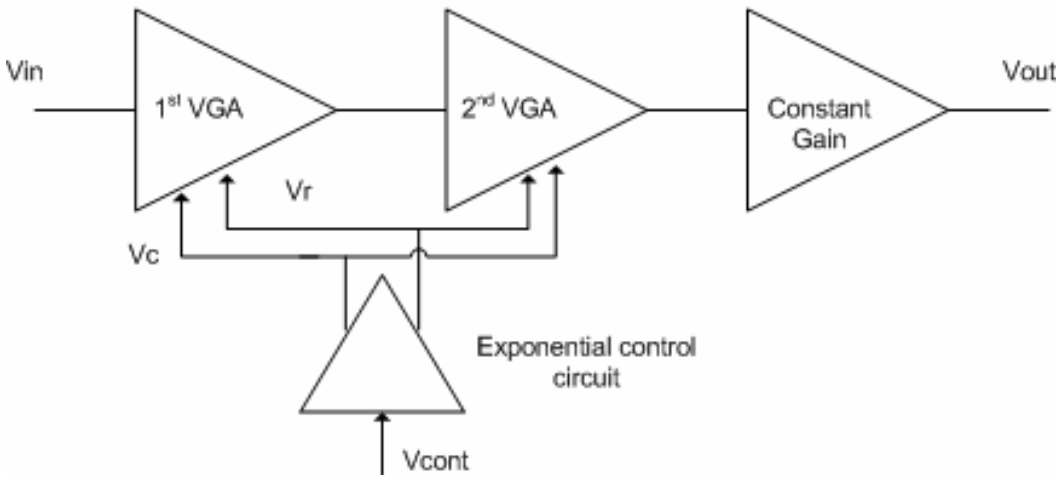


Fig. 6.12 Block diagram of the 3-stage VGA

As illustrated in Fig. 6.13, the current steering topology is implemented in the first two stages for high linearity. The stage gain is then tuned by both control signals, Vr and Vc in Fig. 6.13, simultaneously. In addition, the internal gain control signals (Vr and Vc) are generated from the exponential control circuit shown in Fig. 6.14. As a consequence, the linear-in-dB variable gain characteristic is realized in the overall VGA by combing the current steering stage and the exponential control block.

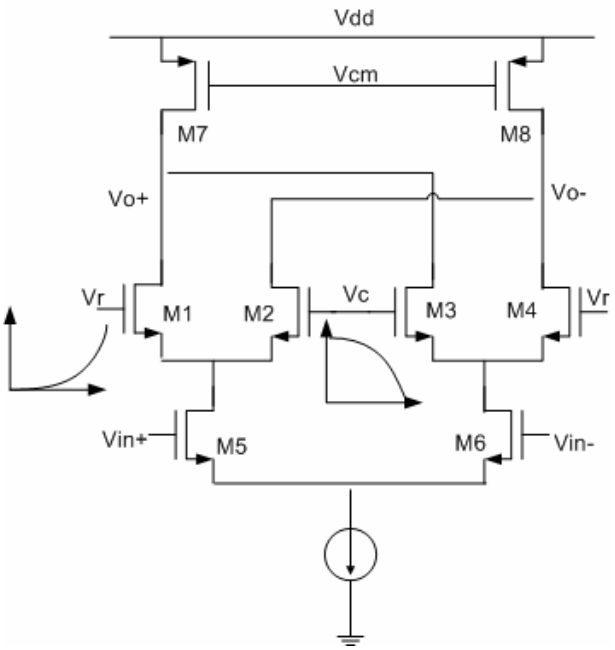


Fig. 6.13 Schematic of the current steering variable gain stage

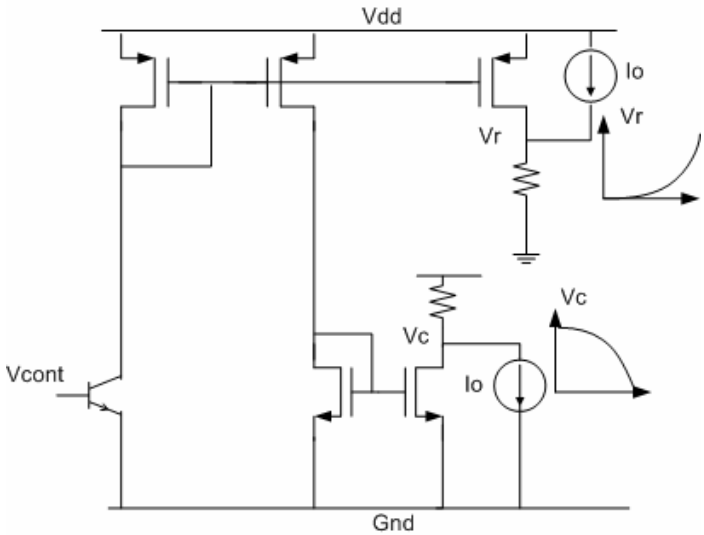
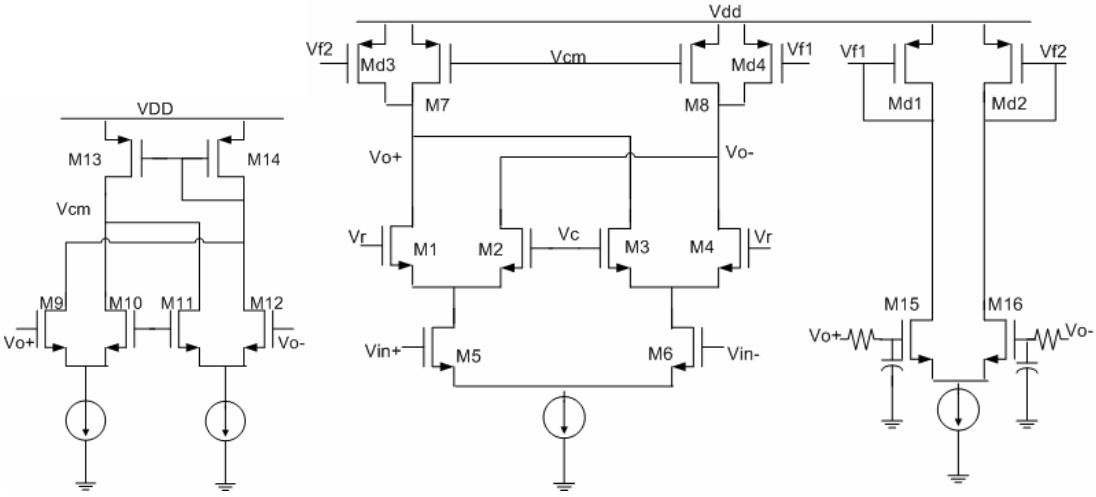


Fig. 6.14 Schematic of the exponential control circuit

Moreover, common-mode feedback and DC-offset cancellation circuitry [6] are also included in the first two stages, which are shown in Fig. 6.15 (a), and (b) respectively. The common output DC from each stage is sensed and compared with a reference voltage. The amplified feedback signal is connected to the gate of PMOS load transistors, M7 and M8, by Vcm. In contrast, in the DC offset cancellation loop, the differential DC signals are first retrieved by two RC filters as shown in Fig. 6.15 (b). Two feedback signals, Md1 and Md2, are generated to fine tune the differential DC outputs through the control of a small portion of the PMOS load transistors (Md3 and Md4).



(a) (b)

Fig. 6.15 Schematic of (a) common mode feedback circuit, and (b) DC offset cancellation circuit

6.4.2 Measurement Results of the VGA

Operated from 1.8-V supply, the I- and Q-channel VGAs dissipate a total current of 28 mA, and measure a highest gain of larger than 60 dB. Fig. 6.16 shows the measured overall gain versus control voltage plot, which roughly appears in

linear-in-dB as expected. Moreover, the lowest achievable gain is much lower than the specified minimum gain of 10 dB. The AC response at different gain scenarios is described in Fig. 6.17. The -3 dB bandwidth at 55 dB gain case is observed to be around 350 MHz, which is already wide enough to cover the desired bandwidth. In addition, an output 1-dB compression point of 8 dBm is measured as well, which is plotted in Fig. 6.18. Table 6.4 summarizes the measured performances of the VGA.

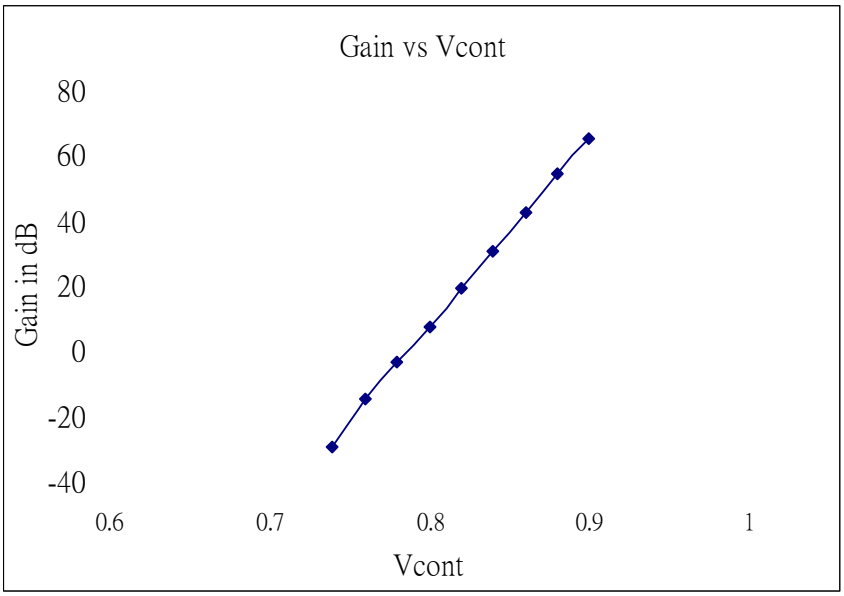


Fig. 6.16 Gain versus control voltage plot of the VGA

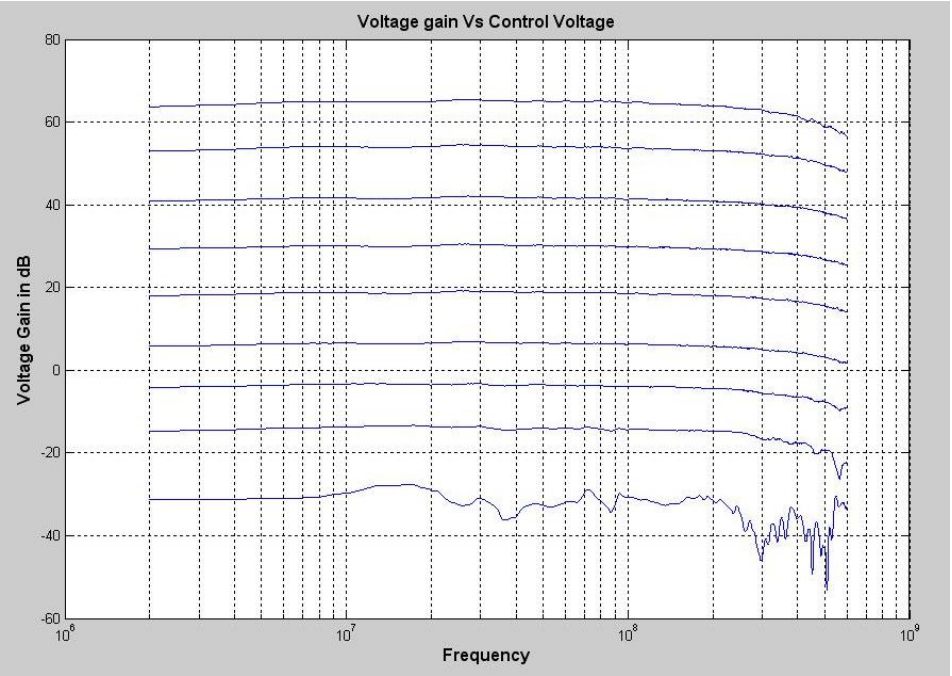


Fig. 6.17 AC response of the VGA at different voltage gains

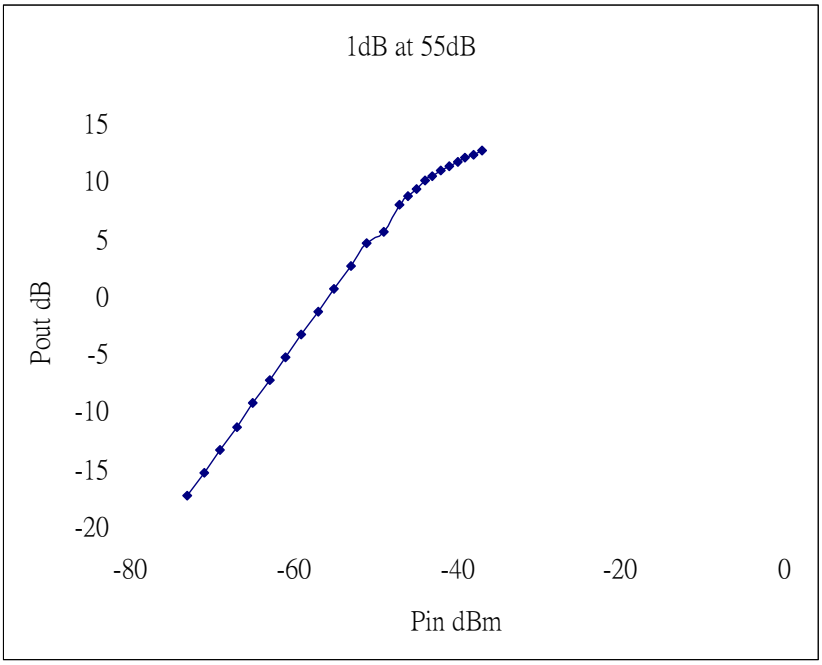


Fig. 6.18 Output P-1dB plot of the VGA at 55 dB gain

Table 6.4 Performance summary of the VGA

Supply	1.8 V	Power consumption (mA)	28 mA (IQ)
IIP3 (dBm)	19 dBm@55dB	OP-1dB	8 dBm
NF (dB)	13.8 dB@55dB	-3dB Bandwidth	350 MHz
Variable Gain (dB)	10 ~ 60 dB		

6.5 ADC

6.5.1 Design of the ADC

The 6-bit ADC in the UWB receiver is predicted to process an input signal bandwidth from 2MHz to 264MHz with a sampling clock frequency of 528MHz. Such kind of ADCs can be implemented with flash type [7]-[8] due to its higher sampling frequency compared with other types. However, for 6-bit resolution, a flash architecture needs $2^{\wedge 6}$-1=63 comparators. Accordingly, a large number of pre-amplifiers are needed even though interpolating is implemented. The huge power consumption is expected for large number of devices as well as the clock distribution circuitry. On the other hand, a two-step sub-ranging architecture can achieve the same resolution with smaller hardware cost. But the speed can not be that high. That is because the input signal needs to be digitalized, reconstructed to analog domain before the residue signal can be generated. These serial operating actions need to be completed in half clock cycle. Therefore, a sampling frequency of 500 MHz is difficult to achieve by this architecture.

In contrast, Folding and Interpolating architecture can reduce the number of comparators. For 6-bit resolution, by using a fine ADC for 4LSBs and a coarse ADC

for 2MSBs, the total number of comparators is 18. The number of gain stage units is also smaller than that of the flash architecture. Meanwhile, this architecture is a parallel architecture, i.e. the coarse and fine conversions are operating in the same clock period. Therefore the speed can be comparable with the flash architecture.

The proposed folding and interpolating ADC consists of a coarse converter and a fine converter operated in parallel to achieve comparable speed with flash ADCs [9]. However, as in flash ADCs, the folding amplifiers and the comparators introduce a large input-referred offset which limits the resolution that the ADC can achieve. In order to suppress the offset, it is necessary to add low-offset pre-amplifiers before the folding amplifiers.

Fig. 6.19 presents the block diagram of the proposed folding and interpolating ADC. The input signals and the reference voltages generated by a resistor ladder are connected to 20 pre-amplifiers, which are followed by a distributed track-and-hold (T/H) circuit. The outputs of T/H circuit are then connected to four folding amplifiers, each of which consist of 5 differential pairs sharing the same resistor load. Moreover, interpolation networks with an interpolation factor (F_F) of 4 are implemented by poly resistors at the output nodes of the folding amplifiers. An array of 16 comparators is connected to the outputs of the folding amplifiers to generate 16 digital outputs which form the ADC's 4 LSB outputs. Finally, the outputs of the comparators are combined with the outputs of a coarse 2-bit ADC by the digital encoder to obtain the final binary output bits.

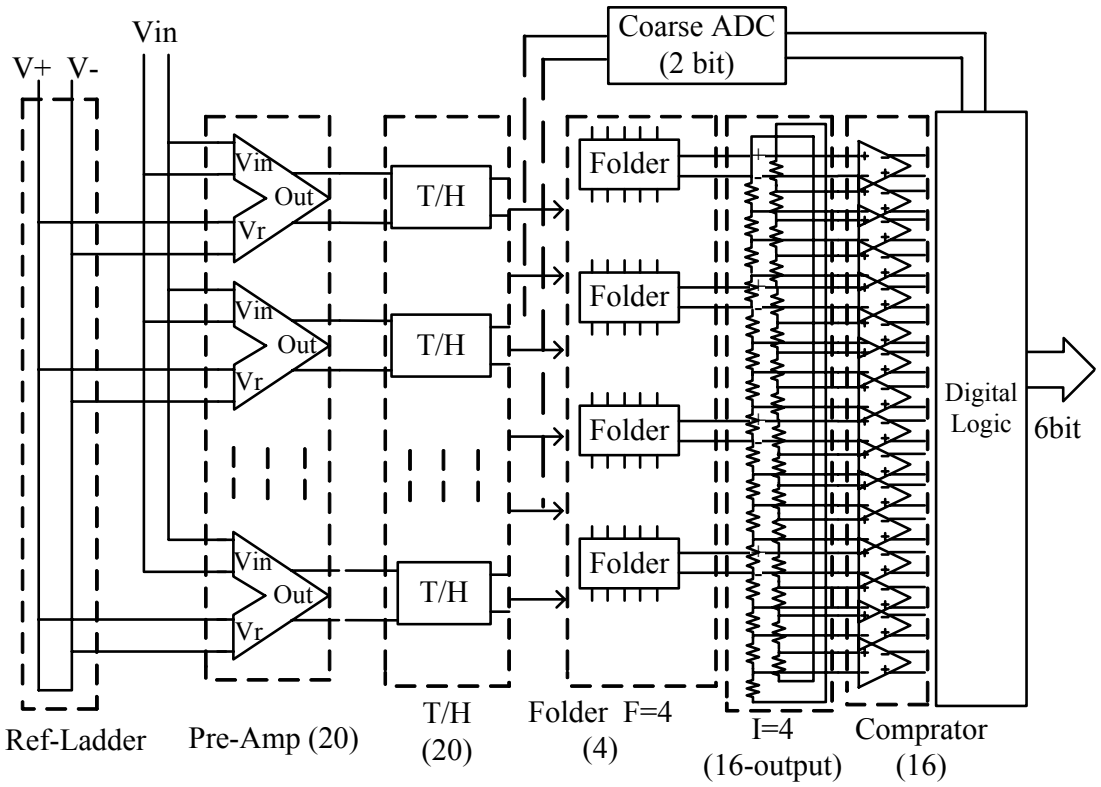


Fig. 6.19 Block diagram of the proposed folding and interpolating ADC

Pre-amplifier is an essential part to suppress the offset from latter stages and it is widely used in flash ADCs and folding and interpolating ADCs. To reduce the offset of the pre-amplifiers, AC coupling capacitors and bias resistors with differential reference voltages are implemented as shown in Fig. 6.20. With this modification, only one differential pair is needed for signal combination, which results in lower offset, lower power, and higher operation frequency. The low-corner frequency formed by the AC coupling capacitor and the resistor is designed to be 2 MHz since the DC carrier is not used in the UWB systems.

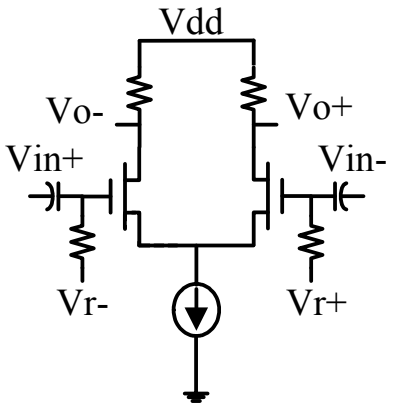


Fig. 6.20 Schematic of the proposed pre-amplifier

As shown in Fig. 6.19, distributed T/H circuit instead of a front-end one is implemented. In this way, the accuracy requirement of T/H circuit is relaxed by the gain of pre-amplifier. Furthermore, linearity requirement is also alleviated since the T/H circuit does not need to cover the whole dynamic range. As shown in Fig. 6.21 (only single-ended version is shown for clarity), the T/H circuit consists of a sampling switch (M_{sample}), a sampling capacitor (C_{sample}), and a dummy switch (M_{dummy}) to minimize the clock feed through and charge injection effect.

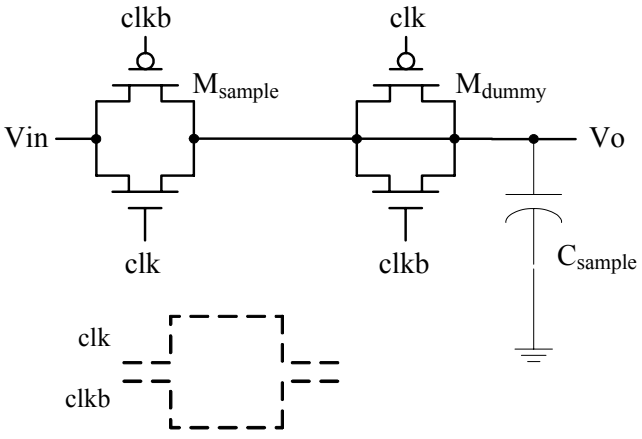


Fig. 6.21 Structure of the T/H circuit

The design of the folding amplifier is conventional, which consists of 5 differential pairs including one dummy pair [10] as shown in Fig. 6.22. Fig. 6.23

shows the conventional structure of the comparator [11] consisting of a pre-amplifier, a latch, and an output buffer.

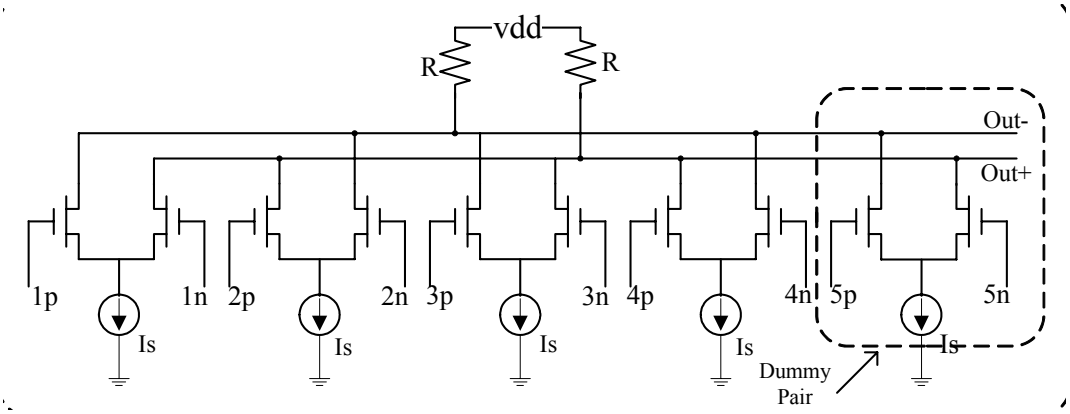


Fig. 6.22 Schematic of the folding amplifier

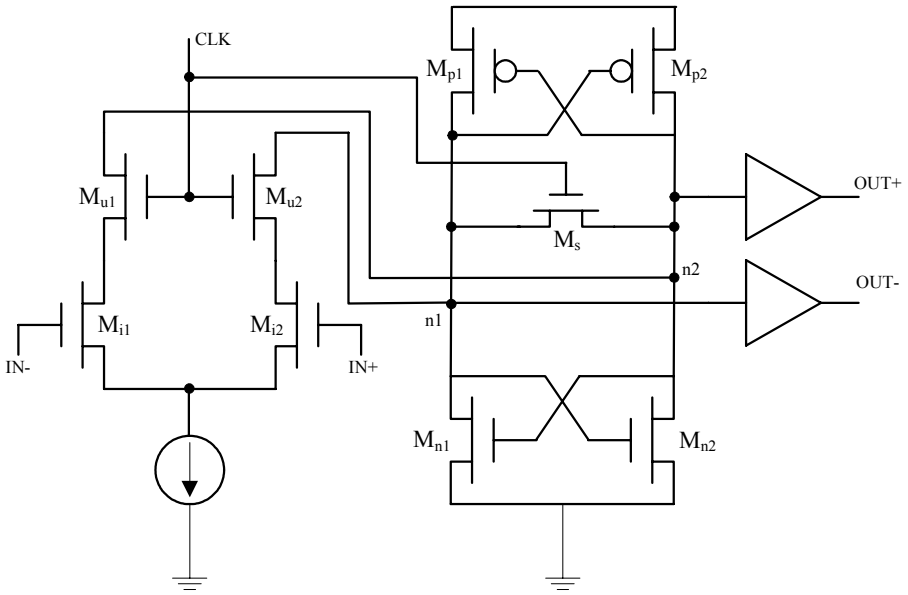


Fig. 6.23 Schematic of the comparator

The block diagram of the coarse ADC is shown in the right part of Fig. 6.24. The second MSB (Bit_4) is determined by the reverse value of the output of the fifth comparator (‘com<4>’) in the fine ADC. The MSB (Bit_5) is decided by a MUX. The control signal ‘ctr’ is the XOR of the two signals ‘C12’ and ‘C8’ which are achieved by the comparison results of the outputs of the 12^{th} and 8^{th} T/H circuits, respectively. If the input is higher than the 12^{th} reference level or lower than the 8^{th},

'ctr' is 0, and MSB equals to 'C8'. On the other hand, if the input lies between the 8th reference level and the 12th reference level, 'ctr' is 1, and MSB equals to 'com<4>'.

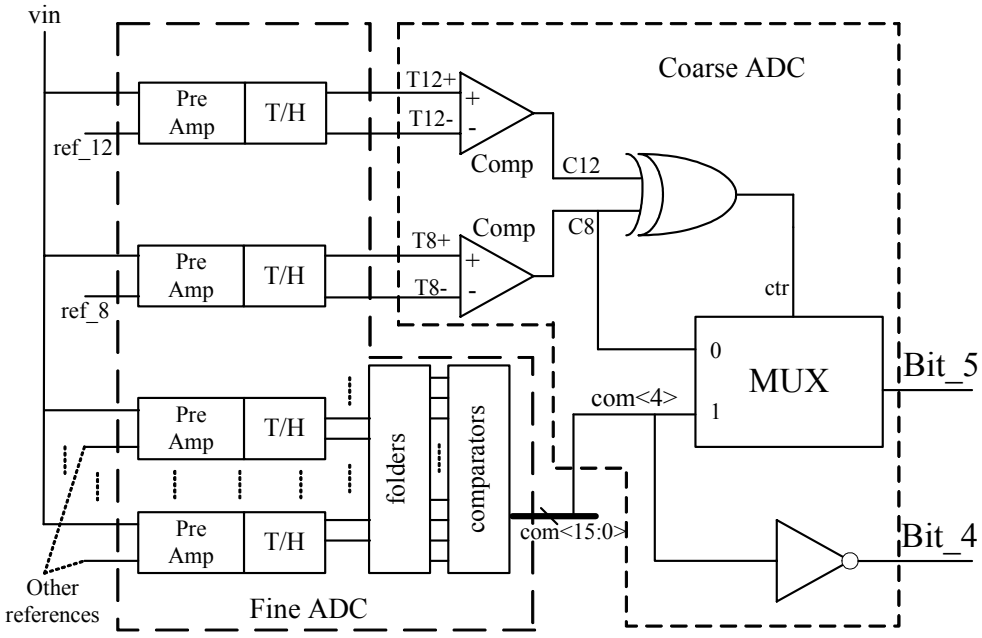


Fig. 6.24 Block diagram of the 2-bit coarse ADC

6.5.2 Measurement Results of the ADC

Operated at 1.8-V supply, the total current consumption for two ADCs (I&Q) is 190mA including 104mA for the analog part and 86mA for the digital part. The input full range is 1.36V which is 75% of the supply voltage of 1.8V. The ADC works properly without implementing calibration and error correction, and achieves SNDR of better than 31.9 dB with an input signal up to 250MHz at the clock frequency of 500 MS/s. Fig. 6.25 shows the FFT plot at 250MHz input of the ADC. Table 6.5 summarizes the performance of the ADC.

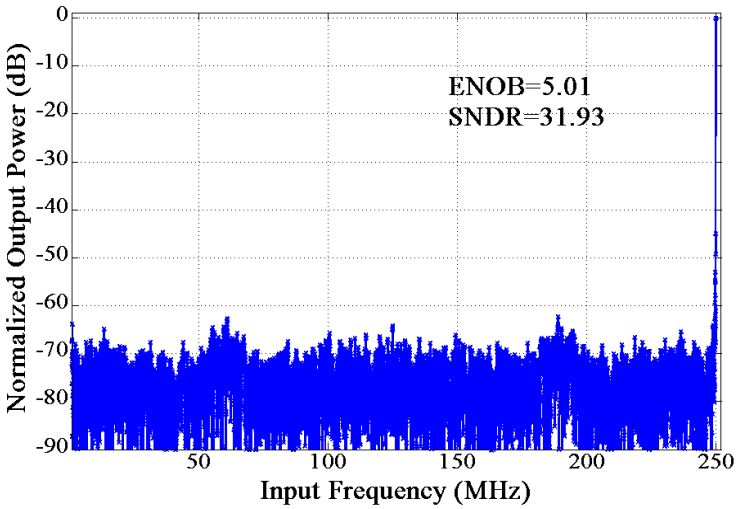


Fig. 6.25 ADC output spectrum with 250 MHz input

Table 6.5 Performance summary of the ADC

Supply	1.8-V	Power consumption (mA)	190 mA (IQ)
Resolution	6-bit	Sampling Rate	500-MS/s
Peak SNDR	33.5dB	INL / DNL	0.7 LSB / 0.4 LSB

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Chapter 7 INTEGRATION AND MEASUREMENT OF THE UWB TRANSCEIVER

7.1 Transceiver Layout Floor-plan and Considerations

The proposed 9-band UWB transceiver is designed and fabricated in TSMC 0.18-μm CMOS process (V_{Tn} = 0.52 V, V_{Tp} = - 0.54 V) with 6 metal layers. Fig. 7.1 shows the die photograph of the proposed transceiver for 9-band MB-OFDM UWB systems.

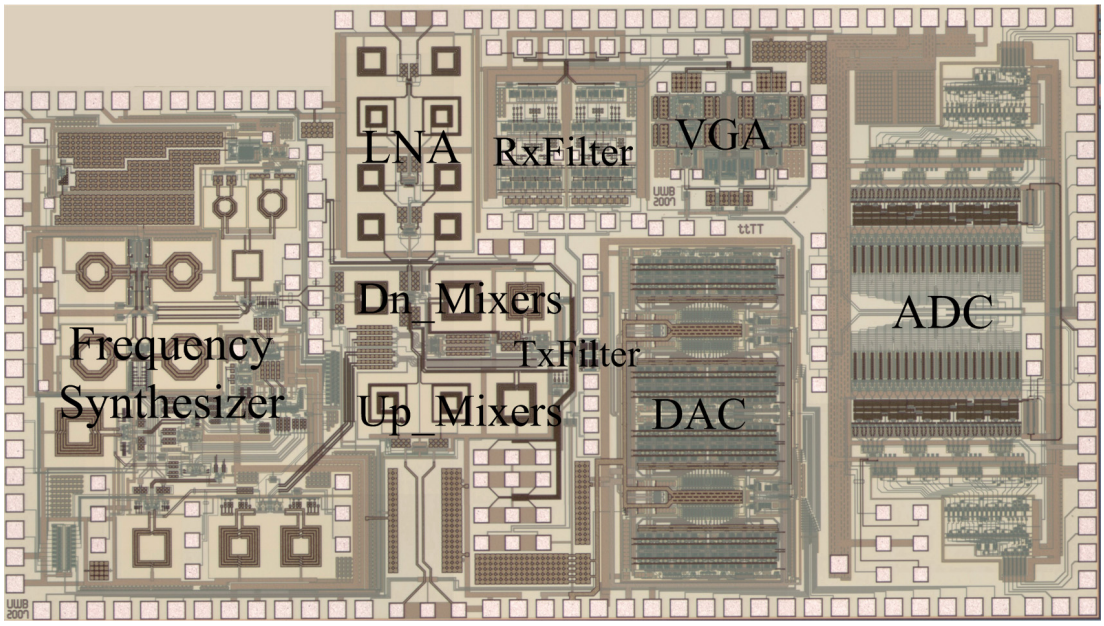


Fig. 7.1 Die photograph of the transceiver for 9-band MB-OFDM UWB systems

Due to the high frequency transmission of the signals inside the transceiver, the transceiver's performances will be largely layout dependent. Therefore, as shown in Fig. 7.2, careful layout floor-plan is necessary to minimize the effects from the parasitic resistances, capacitances and inductances as well as the mismatches.

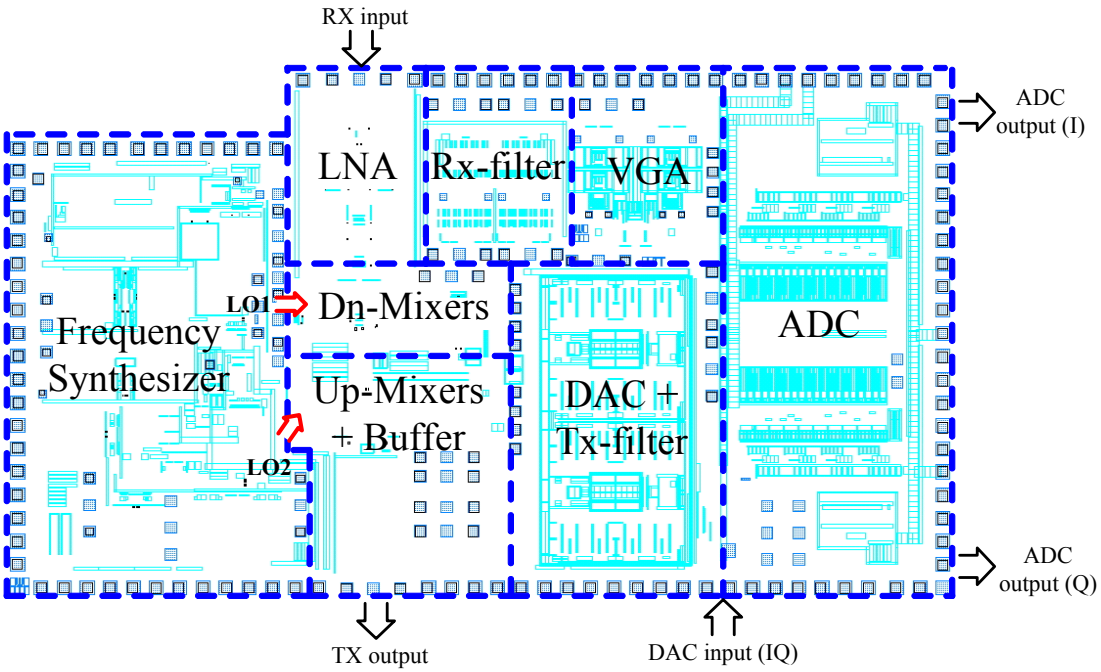


Fig. 7.2 Layout floor-plan of the UWB transceiver

One of the most critical points in the fully-integrated transceiver is the interconnections between the synthesizer and the mixers including the upper-conversion mixers and the down-conversion mixers. On the one hand, the synthesizer occupies the largest chip area, which makes a longer driving line potentially. On the other hand, the first LO1 signal has higher frequency of up to 10.6 GHz. The LO2 frequency is relative lower; however, good matched IQ outputs are desired. To address these issues, the synthesizer is placed at the left side of the whole transceiver layout. In addition, the distance of the interconnection between high frequency LO1 and its mixers is minimized. The IQ signal lines from LO2 need to go a longer way, but they are well matched with carefully layout.

Another critical issue in the fully-integrated transceiver is the substrate coupling between the digital part and the analog part. To minimize the coupling from the ADC and DAC to the other analog circuits, the ADC and DAC blocks are located at the

right side of the chip. Furthermore, in addition to the guard ring surrounding the ADC and DAC, an extra wide guard ring with a width of 100μm is inserted between the analog and the digital blocks to bypass the digital noise.

At last, internal pads consisting of high-impedance pads and SGS pads with an open-drain buffer are included to check the performance of each building block inside the transceiver as well as the output from some critical points.

7.2 Inductor and Transformer Measurement

Because of the high frequency signals in the UWB transceiver, lots of inductors and transformers are needed in the synthesizer, LNA and mixer as well. During the design stage, the inductors and transformers are simulated and modeled using Momentum from ADS. Further step verification is then performed with the on-wafer measurement of the inductors and transformers from separated testing structures.

7.2.1 Setup and Calibration

On-wafer testing structures are usually realized by placing the device under test (DUT) with one or two GSG pads, keeping interconnection lines as short as possible to allow probing with GSG RF probes [1]. A typical example is the center-tapped inductor testing structure shown in Fig. 7.2. One GSG pad is employed to measure the one-port S-parameter of the inductor, in which one terminal of the inductor is connected to the signal-pad, while the other terminal is shorted to the ground-pad. It is clear from the layout that, apart from the signal-pad capacitance, the interconnections to the inductor will affect the measured impedances and hence

accurate de-embedding will be required. Therefore, to characterize the parasitic capacitance and inductance from the GSG pad and interconnections, two more testing structures with open and short configurations are implemented. Consequently, a two-step "open-short" de-embedding scheme [2] is applied to retrieve the pure S-parameter of the inductor.

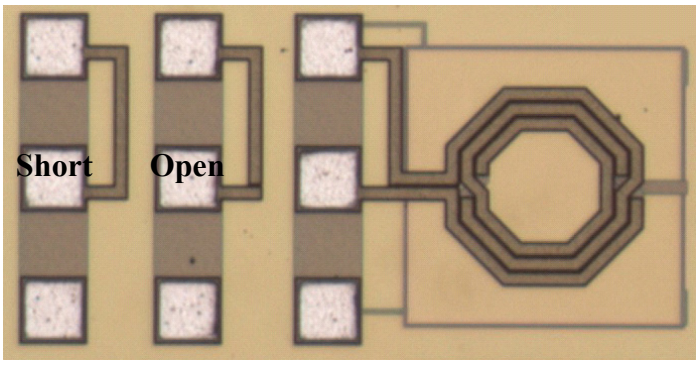


Fig. 7.3 Layout of an on-wafer inductor testing structure with one-port GSG configuration

In the two-step open-short de-embedding approach, it is assumed that all the parallel parasitics are located in the signal-pad and all the series parasitics in the interconnection lines. The corresponding equivalent circuit is depicted in Fig. 7.4.

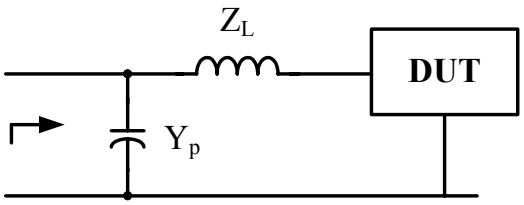


Fig. 7.4 Equivalent circuit model used for the two-step correction method

To enhance measuring accuracy, the two-port calibration with an impedance standard substrate is first performed. The parasitics surrounding the inductor is characterized by measuring the 'open' interconnection pattern and the 'short' pattern. This measurement provides us with the 'open' Y-parameter Y_{open}; as well as a

corresponding 'short' Y-parameter Y_{short}. The series impedances can now easily be found from the short measurement with some simple corrections from the open measurement, which is given by

$$Z_L=(Y_{short} - Y_{open})^{-1} \quad (7.1)$$

The actual Z-parameter of the inductor can be obtained from

$$Z_{ind} = (Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \quad (7.2)$$

where Y_{DUT} is the measured Y-parameter matrix of the inductor together with all the parasitics.

In contrast to the inductor, two SGS pads are used in the transformer testing structure, as shown in Fig. 7.5. Full two-part measurement is hence necessary to achieve the pure S-parameter of the transformer. Similar to the measurement performed for an inductor, two-step "open-short" de-embedding scheme is applied with the aforementioned procedure.

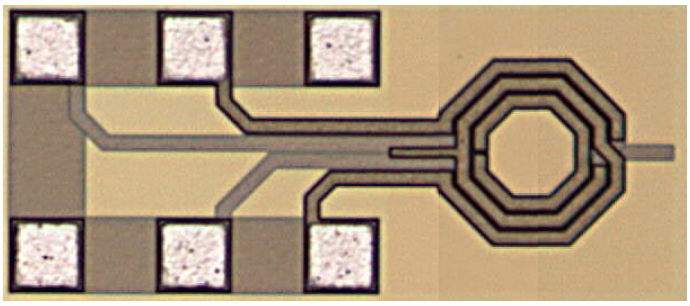


Fig. 7.5 Layout of an on-wafer transformer testing structure with two-port GSG configuration

7.2.2 Measurement Results and Modeling

In our design, ADS simulation is performed to fit the S-parameter of the model into our measured S-parameter by selecting appropriate parameters of the elements in

the model. Fig. 7.6 shows the model of the center-tapped inductor consisting of physical inductance in series with resistance, parasitic capacitance and substrate resistance, which is used in the ADS simulation.

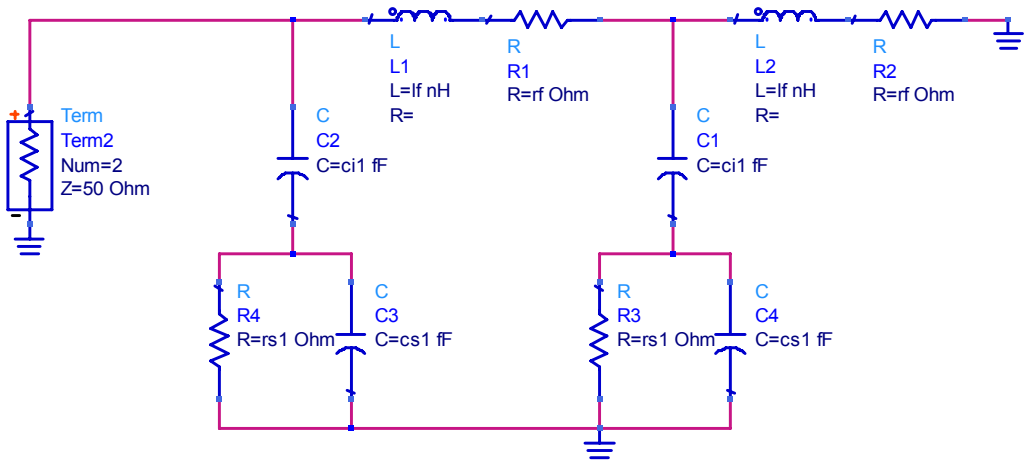


Fig. 7.6 Fitting model of the center-tapped inductor used in the ADS simulation

Tables 7.1 and 7.2 summarize both simulated and measured results of two inductors in the frequency synthesizer for comparison. The 4.2GHz inductor is used in the 1st stage divider of the synthesizer, and the 2.9GHz inductor is included at the LO2 divider stage. The measured inductance value is actually close to the simulation.

Table 7.1 Comparison of the simulated and measured results for the 4.2 GHz inductor

Ind_4.2G	Lf (n)	Rf (ohm)	Ci (fF)	Rs (ohm)	Cs (fF)	Q (4.2G)
Sample1	1.03824	1.26	316.552	729.192	64.7734	8.11
Sample2	1.0397	1.1889	322.223	733.51	62.9062	8.269
Sample3	1.0373	1.179	320.453	726.84	63.75	8.28
Simulation	1.161	1.38	61.3	129	253.8	
Frequency	3 ~ 6 GHz					

Table 7.2 Comparison of the simulated and measured results for the 2.9 GHz inductor

Ind_2.9G	Lf (n)	Rf (ohm)	Ci (fF)	Rs (ohm)	Cs (fF)	Q (2.9G)
Sample1	2.1084	2.2678	266.15	798	266.15	7.3
Sample2	2.1062	2.2919	243.66	800	120.336	7.538
Sample3	2.0961	2.2255	284.04	800	114.84	7.122
Simulation	2.36	4	70.16	205.78	382.63	
Frequency	1 ~ 4 GHz					

The fitting model of the transformer is explained in Fig. 7.7. On top of the magnetic coupling factor of K between the primary coil (L1 & L2) and the secondary coil (L3 & L4) of the transformer, additional capacitive coupling Ck is included in the model.

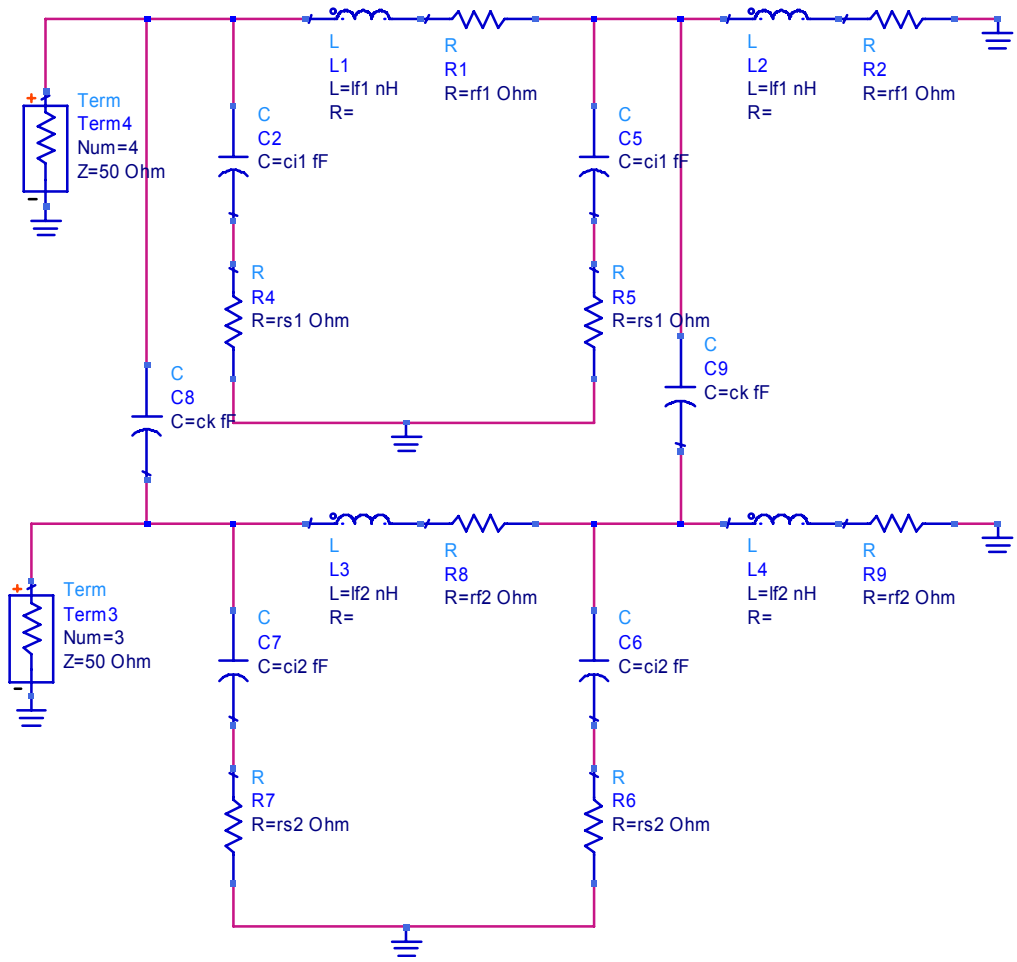


Fig. 7.7 Fitting model of the transformer used in the ADS simulation

The transformer in the QVCO of the synthesizer is measured with a separated testing structure, which is operated at 8.448 GHz. Table 7.3 compares the measured results from three samples with the simulated results in the ADS. The measured magnetic coupling factor of K is around 0.7, which is indeed better than the one from the simulation.

Table 7.3 Comparison of the simulated and measured results for the 8.5 GHz transformer

	Sample 1	Sample 2	Sample 3	Simulation
L1 (nH)	0.4655	0.4967	0.4451	0.481
R1	0.9469	1.1983	1.2143	3
Ci1 (fF)	26.1693	38.6673	10.16	40
Rs1	400	161.071	400	128.5
Q1 (8.45 G)	3.94	4.892	3.81	
K	0.70645	0.6962	0.7117	0.453
Ck (fF)	28.302	60.176	43.257	16.9
L2 (nH)	0.14736	0.1355	0.14535	0.106
R2	1.126	0.45	1.048	0.92
Ci2 (fF)	107.247	112.58	199.88	17
Rs2	50	320.879	237.04	138
Q2 (8.45 G)	2.714	5.116	2.65	
Frequency	6 ~ 11 GHz			

7.3 Receiver Measurement

The receiver performances are characterized with on-wafer probing for the RF input and output signals. Specifically, a SGS RF probe is applied at the LNA input together with an external single-end to differential balun in front of the LNA. Similarly, the analog output signals from the VGA are taken by SGS or High-impedance probing as well.

7.3.1 NF

Noise figure meter HP8970B is used to characterize the NF performance of the receiver. Fig. 7.8 presents the block diagram of the setup including all the component models needed in the measurement. To start with, the self-calibration of the noise figure meter is performed by connecting a noise source in the NF meter loop. Then, the NF of the DUT together with the whole setup is captured. Thanks to the large gain in the receiver chain, the NF contribution of the losses from the cables and components at output side is negligible. However, the gain losses from the cables, splitter, and bias-T before the LNA will contribute to the total displayed NF directly, which is hence needed to be de-embedded. To deal with, the total losses previous to the LNA are measured by connecting the input cable from the LNA to the NF meter. As a consequence, the net NF of the receiver is achieved by subtracting the losses from the overall NF.

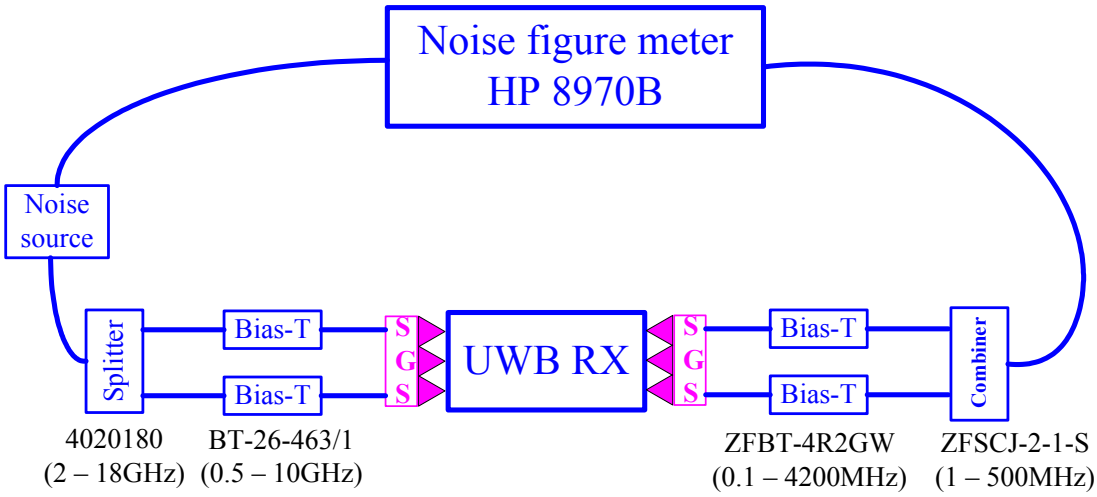


Fig. 7.8 Block diagram of the testing setup for the receiver NF measurement

Fig. 7.9 plots the measured NF of the receiver (including the off-chip single-end-to-differential balun) after calibration under the maximum gain setting for

different bands. A minimum NF of 6.5 dB is achieved at the highest band, while the maximum NF of 8.25dB is observed at the lowest band. There are two main reasons those make the NF at lower frequency band worse than higher band: Firstly, as presented in Chapter 6, the measured NF of the LNA at the lowest band is already 1 dB larger than the highest band; Secondly, the filtering at the output of the LNA is not sharp enough to filter out the noise at image frequency for low frequency bands before down-conversion, so that more noise is added to the input of the down-conversion mixer.

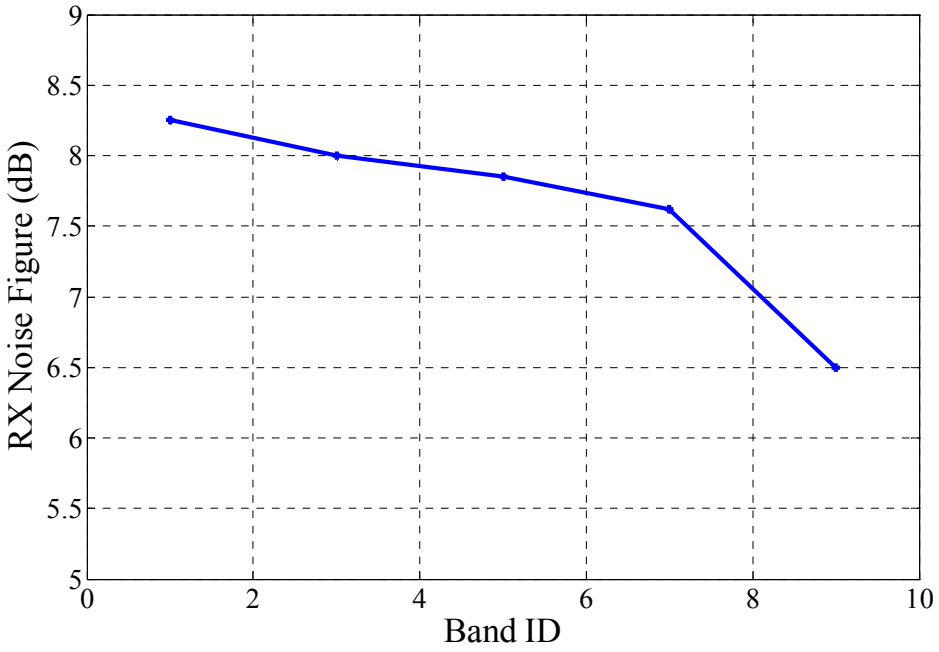


Fig. 7.9 Measured NF of the receiver at different bands

7.3.2 Gain

The receiver gain is measured with single-tone signal at the LNA input. As described in Fig. 7.10, Agilent 8247C signal generator is applied to deliver the required signal; the output signal is then analyzed by Agilent E4440A spectrum analyzer. To find out the receiver gain, all the losses caused by the setup and the

open-buffer are calibrated. As shown in Fig. 7.11, the receiver measures a total of 58.7 dB voltage gain range from 25.3 to 84.0 dB.

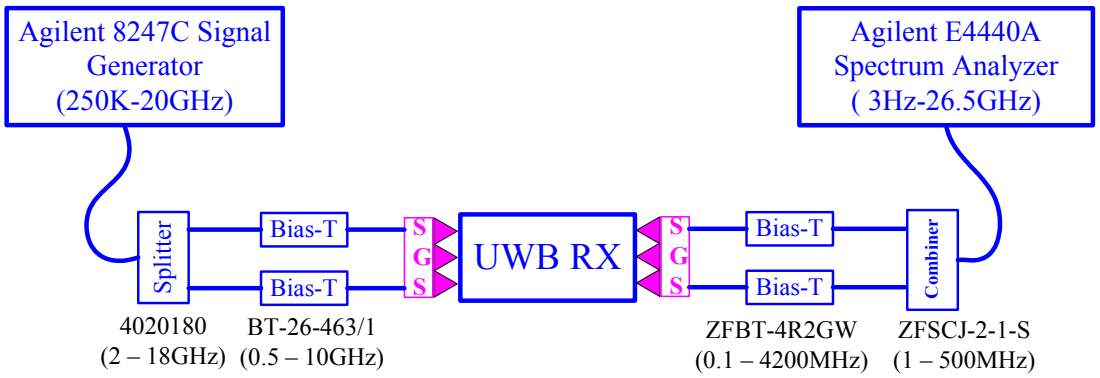


Fig. 7.10 Testing setup for the receiver gain measurement

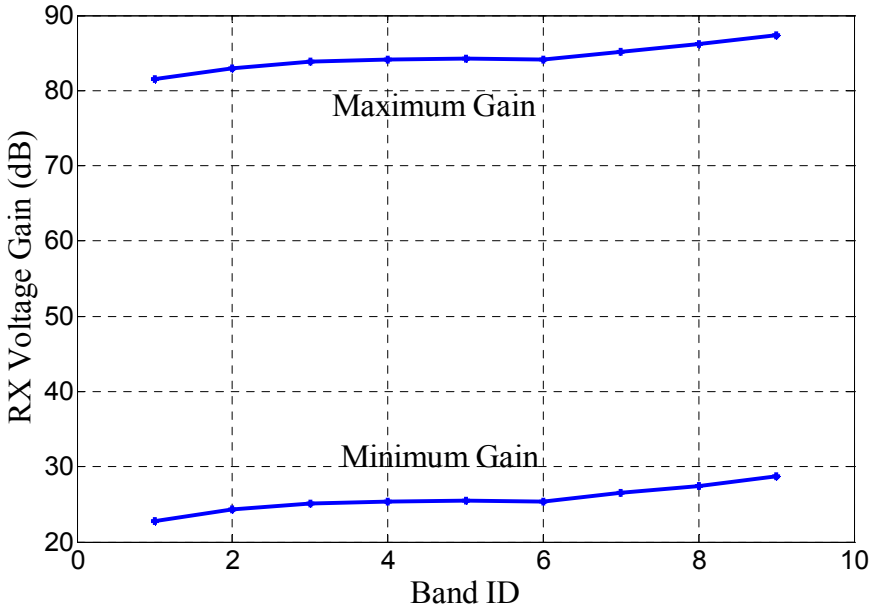


Fig. 7.11 Measured receiver gain range

7.3.3 Input P-1 dB

With the same setup shown in Fig. 7.10, the input-referred 1-dB compression point of the receiver is measured by increasing the input power continuously. A total of three different input frequencies located at low, middle and high bands respectively, is applied to verify the P-1dB performance of the receiver at the lowest gain, which are summarized in Table 7.4. As plotted in Fig. 7.12, the observed

input-referred P-1dB at the 2nd band is -19.9 dBm.

Table 7.4 Measured input P-1dB at three different input frequencies

Input frequency	7138MHz	5554MHz	3970MHz
Measured input P-1dB (dBm)	-22.6	-21.7	-19.9

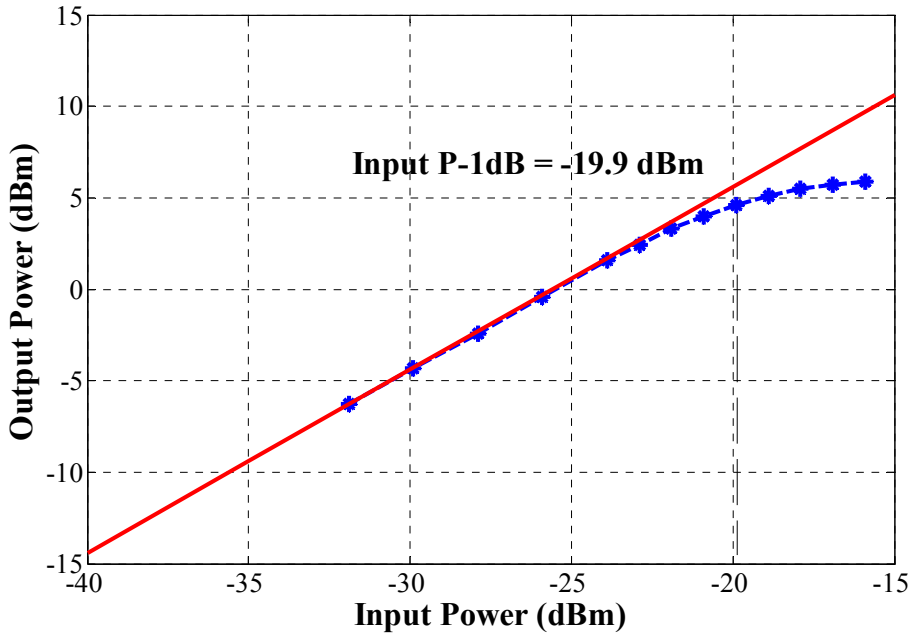


Fig. 7.12 RX input P-1 dB plot at the 2nd band

7.3.4 IIP3

In contrast to the P-1dB testing, two-tone test method is implemented to measure the IIP3 performance of the receiver. Specifically, two tones with channel spacing of few Megahertz are generated from our Agilent E4438C vector signal generator (Frequency range from 250K to 6 GHz), which are presented at the LNA input for in-band IIP3 measurement. With the minimum gain setting of around 26 dB, the receiver measures an in-band IIP3 of -12.65dBm at the 2nd band, and -13.7dBm at the 5th band, respectively. Fig. 7.13 shows the IIP3 plot at the 2nd band.

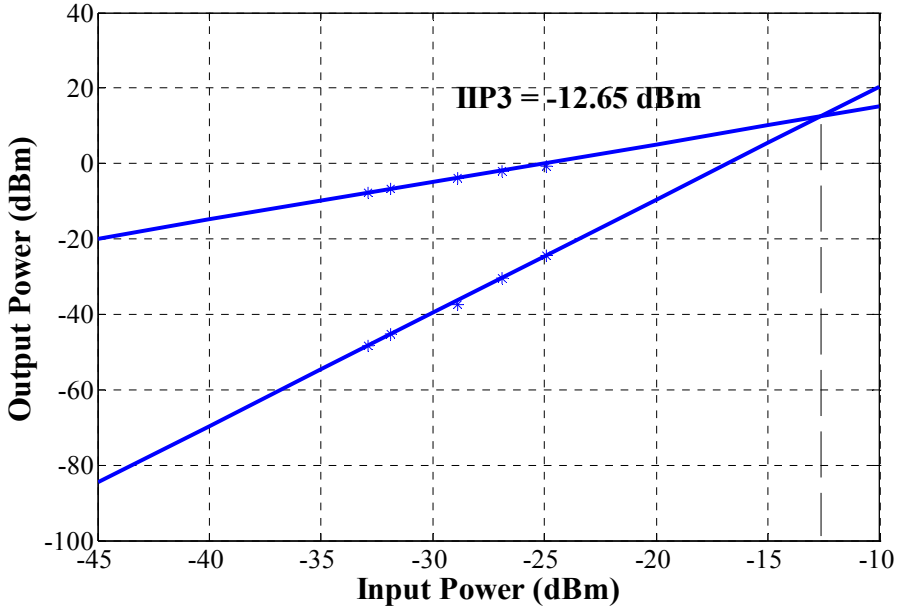


Fig. 7.13 Measured RX IIP3 plot at the 2nd band

7.3.5 IIP2

Two signal generators, Agilent E4438C and Agilent 8247C, are needed to deliver two desired in-band signal tones. Consequently, an in-band IIP2 of around 22 dB is achieved.

7.3.6 Channel Bandwidth and Adjacent-Channel Attenuation

Agilent 8753E (30K-6GHz) network analyzer with frequency offset mode option can be used to measure the AC response of the receiver. As described in Fig. 7.14, the RF input to the LNA is connected to Port 1, while the IF output signal from the VGA is measured by the R-channel input of the network analyzer. Moreover, the LO frequency in the frequency offset mode must be set to the same value as the on-chip LO. Fig. 7.15 plots the measured receiver AC response as a function of the baseband frequency at the 1st band. The receiver chain measures a -10 dB bandwidth of 325 MHz, and an adjacent-channel attenuation of 39 dB at the VGA output.

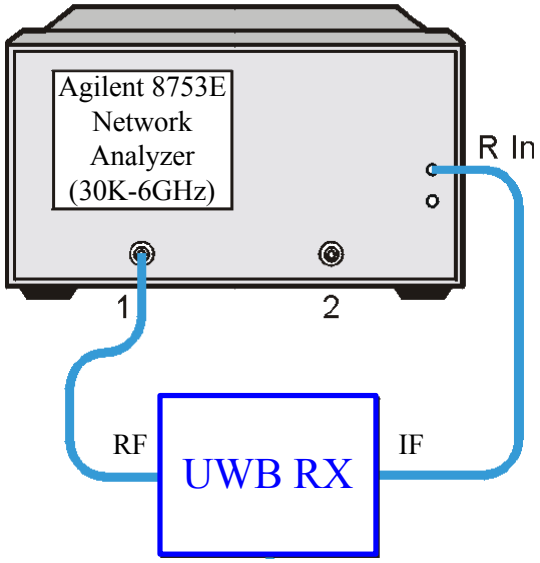


Fig. 7.14 Connection diagram with frequency offset mode measurement

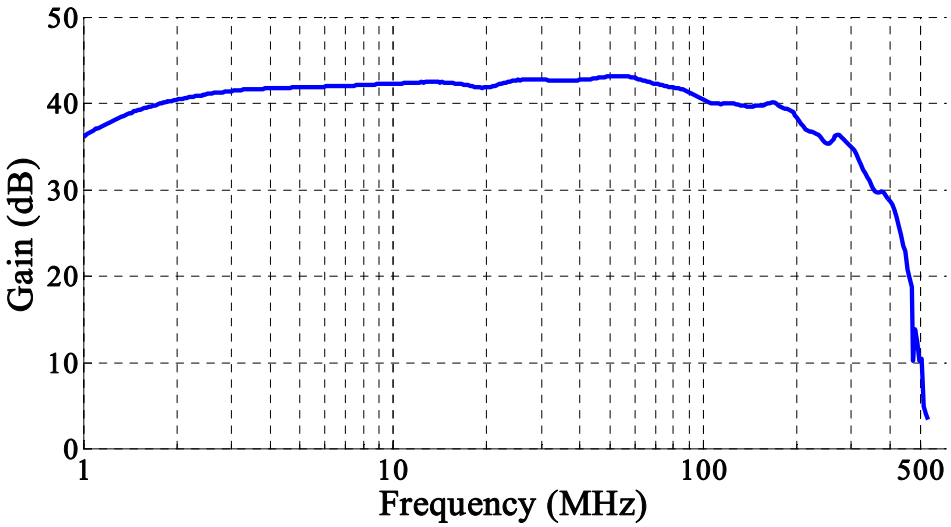


Fig. 7.15 Measured RX bandwidth plot at the VGA output

7.3.7 IQ-Channel Mismatches

Similar to the setup for AC response measurement, a Network analyzer with frequency offset mode is used to verify the IQ-channel mismatches, which is explained in Fig. 7.16. Fig. 7.17 plots the measured IQ phase and gain mismatches of the receiver chain versus the baseband frequency IF2, which are observed to be better than 4 degree and 0.8 dB, respectively.

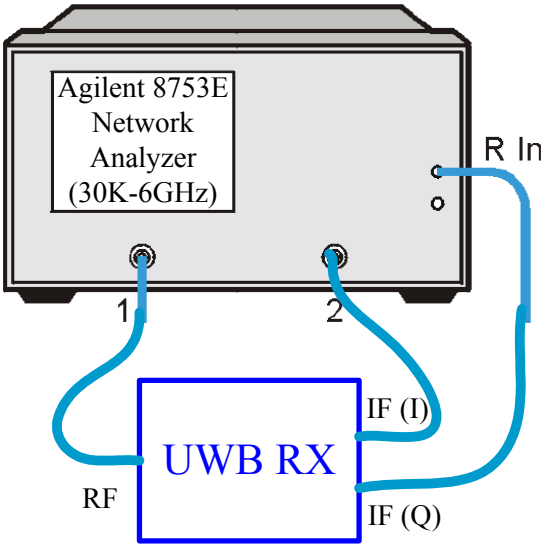


Fig. 7.16 Connection diagram for IQ-channel mismatch measurement

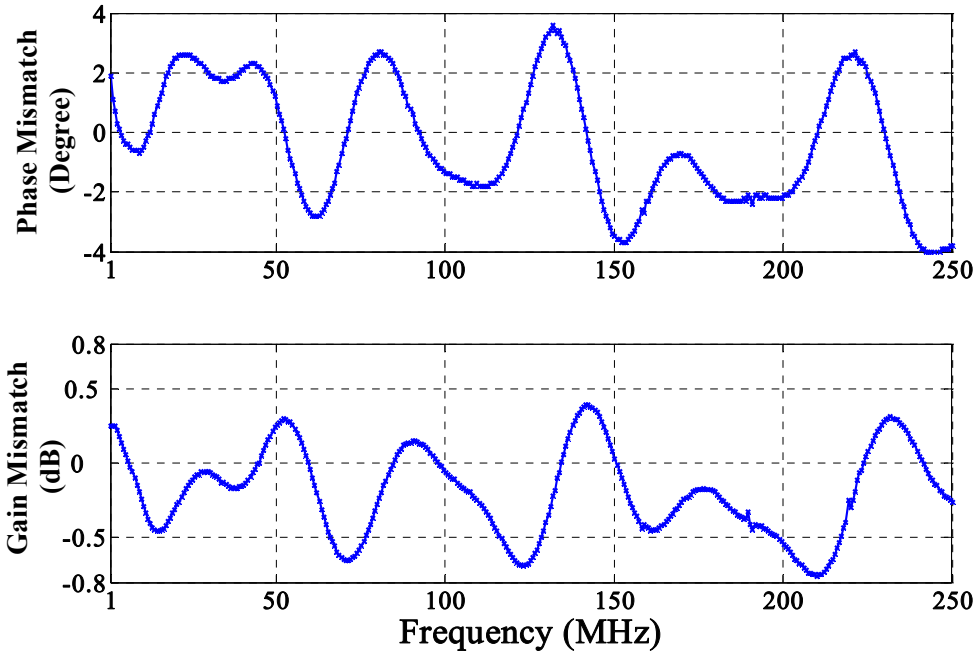


Fig. 7.17 RX IQ path phase & gain mismatch vs. baseband frequency

To give more intuitive impression about the IQ accuracy, Fig. 7.18 shows the IQ-channel time domain waveforms at the VGA output with a baseband frequency of 4 MHz.

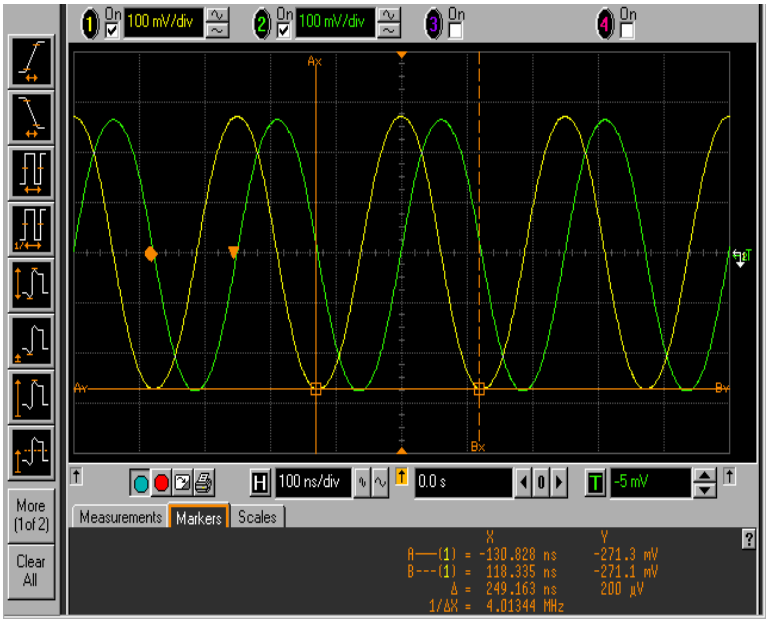


Fig. 7.18 RX IQ-output waveforms at 4MHz

7.3.8 Receiver Sensitivity Without ADC

The receiver sensitivity without the ADC at the highest data rate of 480Mb/s is first studied by measuring the output signal power and noise power at the VGA output. Fig. 7.19 shows the VGA output spectrum for a single tone of -72.3 dBm at the LNA input. The corresponding VGA output noise power is illustrated in Fig. 7.20, which is equivalent to an output SNR of 6 dB.

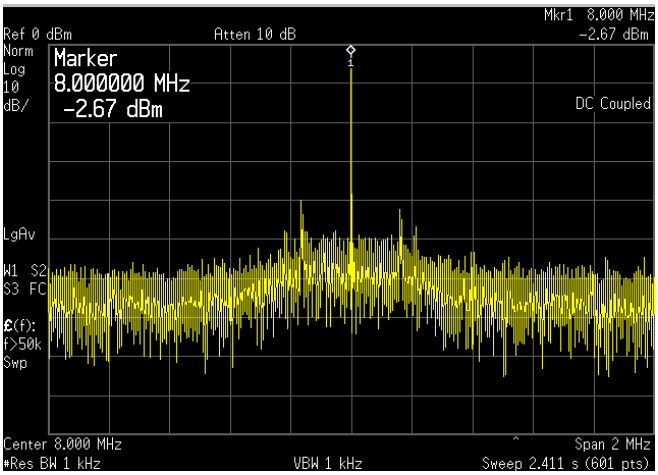


Fig. 7.19 Output spectrum of the signal at the VGA output

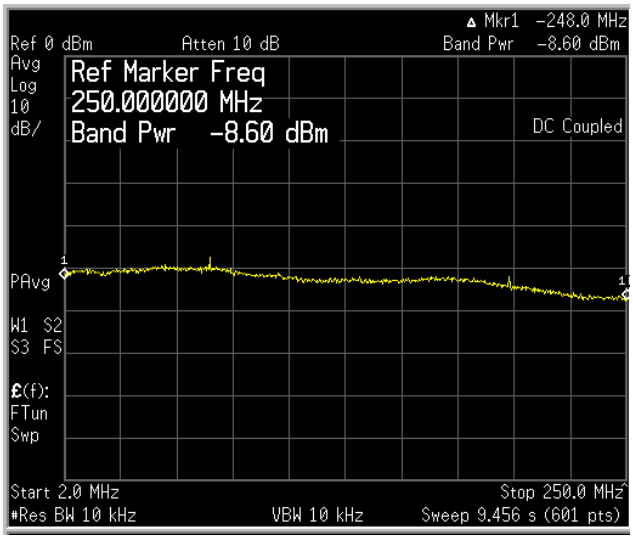


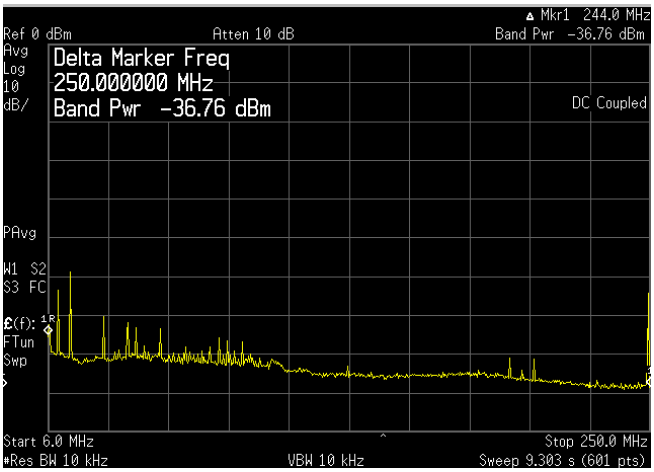
Fig. 7.20 Output noise spectrum at the VGA output

7.3.9 Receiver Sensitivity With ADC

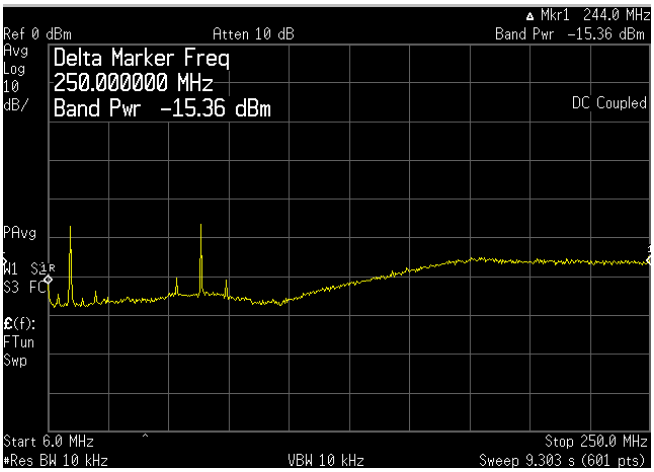
The digital noise coupling existing in a fully-integrated receiver with ADC is a well known problem, as it will decrease the receiver performance significantly. To gain more insight into the coupling effect from the ADC, the VGA output noise spectrum is first plotted. Fig. 7.21 (a) and (b) compare the VGA output noise power for the ADC turn-off and turn-on cases. When the ADC is sampled at a clock frequency of 500MHz, a noise power increase of 21.4 dB is observed at the VGA output for the middle gain setting of the receiver.

To measure the SNR at the ADC output, the digital output signals from the ADC are captured and analyzed by HP 16500B logic analyzer. The ADC is sampled at 500Ms/s by an external clock from HP 80000 data generator. Unfortunately, the best ADC output SNR that we can achieve is around 0.5 dB as shown in Fig. 7.22(a). This is mainly due to the foregoing digital noise coupling from the ADC to the VGA block through the substrate. To give more impression on the digital noise coupling, the ADC output SNR is re-measured as comparison by implementing a lower

sampling frequency clock for a fixed VGA output at 5MHz. As plotted in Fig. 7.22 (a) and (b), the ADC output SNR is improved from 0.5 dB to around 11 dB when the sampling clock frequency is reduced from 500Ms/s to 50Ms/s.

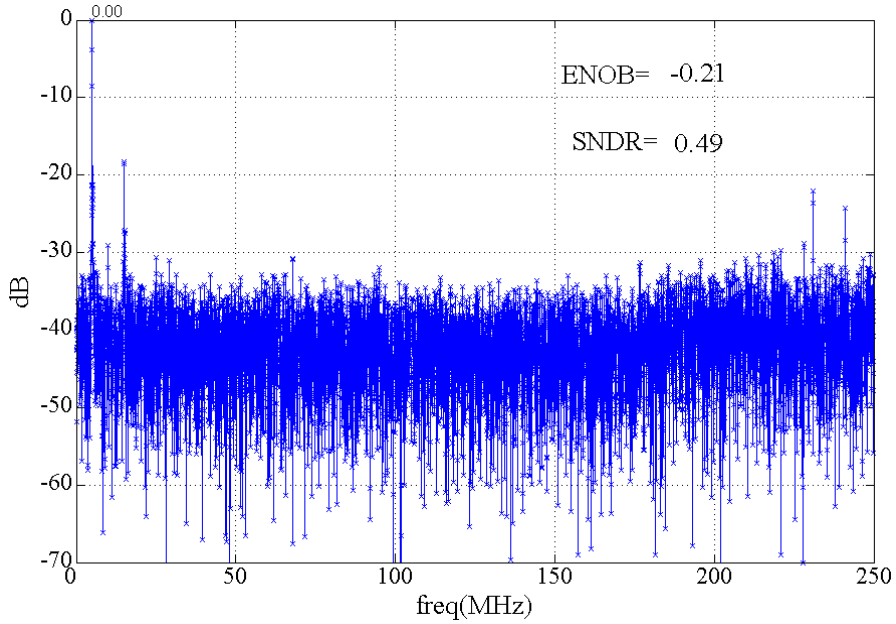


(a) ADC turn-off

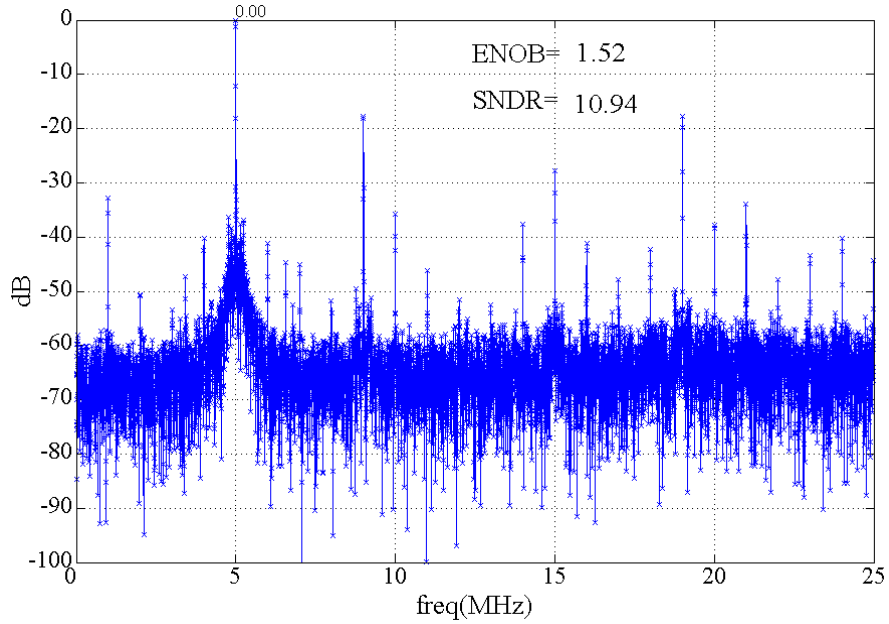


(b) ADC sampled at 500Ms/s

Fig. 7.21 Output noise spectrum at the VGA output (a) with ADC turn-off, (b) with ADC sampled at 500Ms/s



(a) 5MHz input @ 500Ms/s



(b) 5MHz input @ 50Ms/s

Fig. 7.22 Output SNR of the single-chip receiver with the ADC sampled at (a) 500Ms/s (b) 50Ms/s

We are targeting for a single-chip fully-integrated UWB transceiver including ADC and DAC. However, because of the aforementioned noise coupling problem, the ADC output SNR of the single-chip receiver is worst than the expected one. To do further investigation, the receiver is cut into two separated chips: one contains the

RF and analog part, the other one only has the IQ-channel ADCs part. Both chips are glued on the same PCB as illustrated in Fig. 7.23. On-chip bonding is applied to connect the IQ signals from the VGA output buffer to the ADC input.

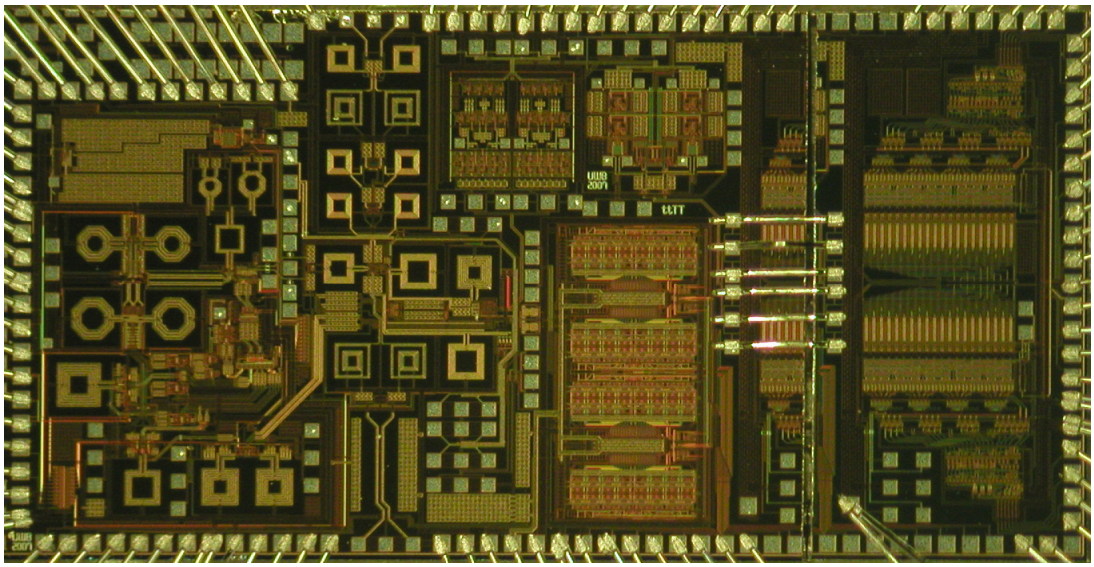


Fig. 7.23 Chip photograph of the two-chip receiver with ADC

With this proposed two-chip solution, the substrate coupling between the ADC and the other analog blocks is eliminated. As presented in Fig. 7.24, the two-chip receiver achieves an ADC output SNR of better than 7.25 dB at the highest data rate of 480Mb/s when a minimum single-tone input power of -69.3 dBm is presented at the LNA input side.

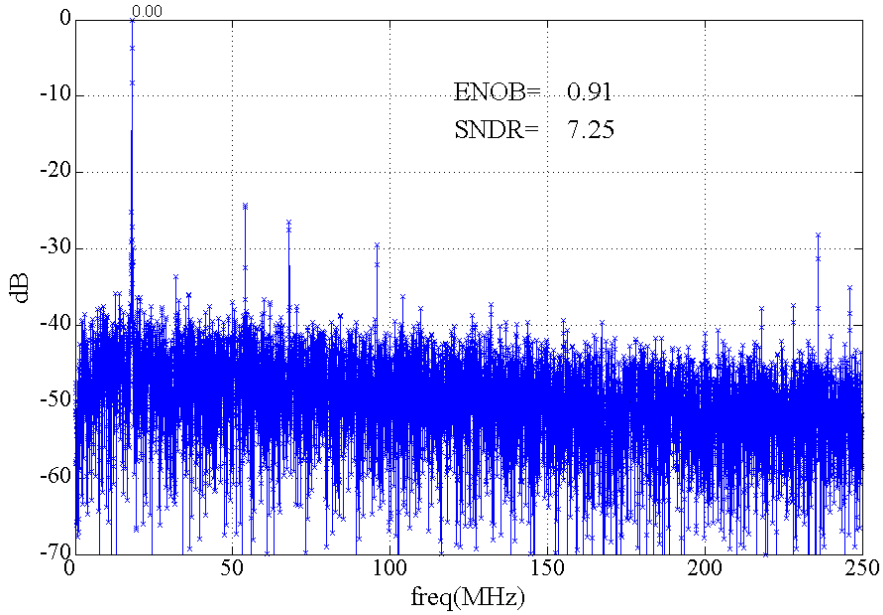


Fig. 7.24 Output SNR of the two-chip receiver with the ADC at 500Ms/s

7.4 Transmitter Measurement

The IQ analog baseband signals for the transmitter are generated from Agilent E4438C vector signal generator. Fig. 7.25 explains the testing setup for the TX measurement.

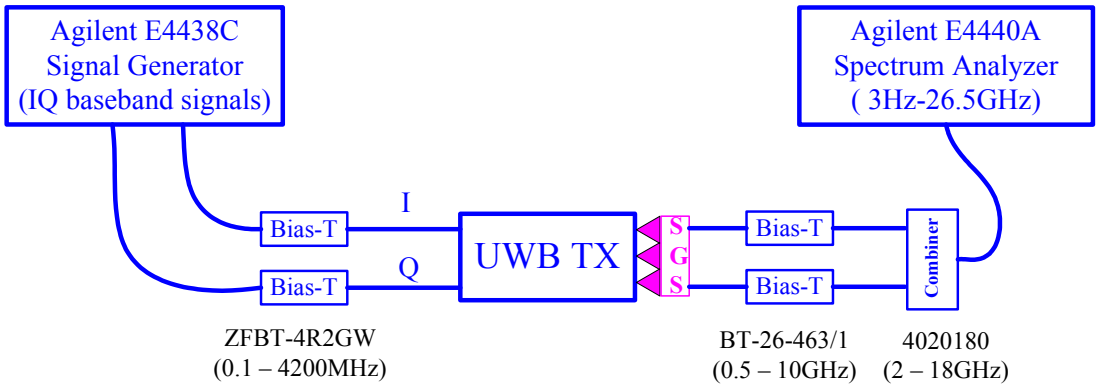


Fig. 7.25 Testing setup for the TX measurement

However, because of the IQ baseband bandwidth limit of the signal generator, the entire TX spectrum mask can not be measured. Hence, the other relevant parameters such as output P-1dB, sideband rejection, LO leakages and so on, are measured to study the preliminary performance of the transmitter.

7.4.1 Output P-1 dB

The TX output P-1dB is measured with a single tone IQ-signal applied at the TX-filter input. As plotted in Fig. 7.26, an output P-1dB of better than -8.2 dBm is measured at the output of the transmitter.

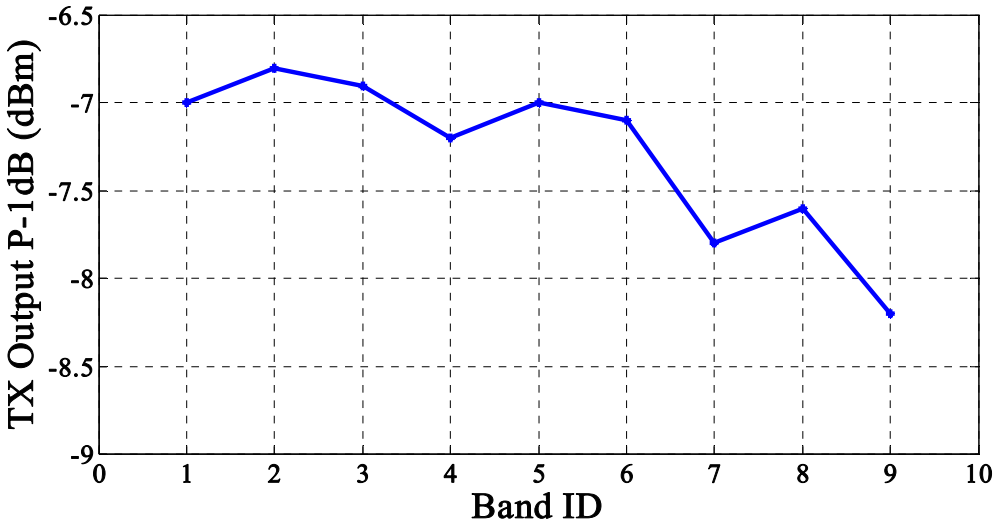
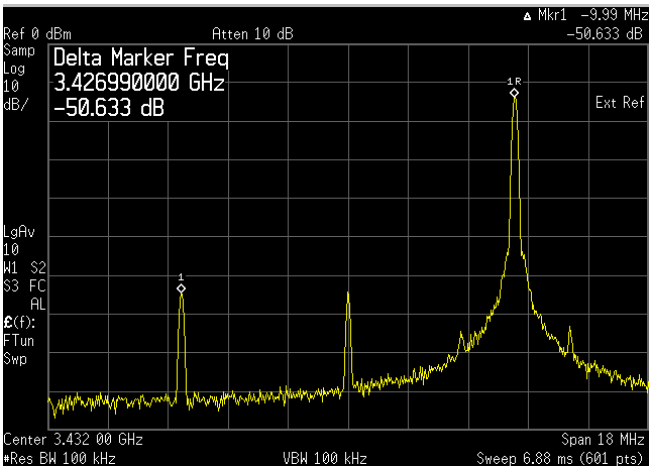


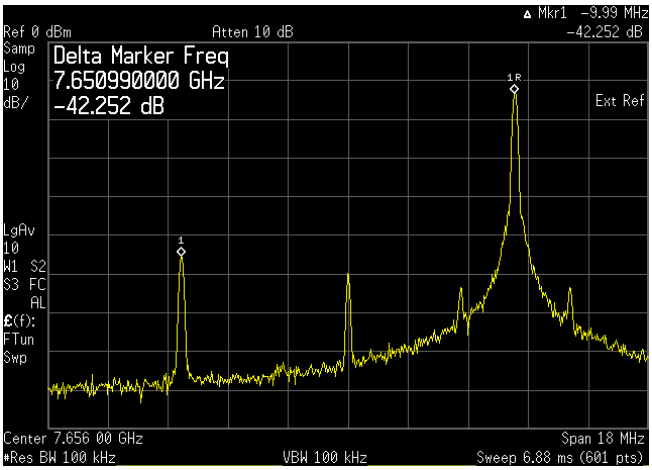
Fig. 7.26 Measured TX output P-1dB at different bands

7.4.2 Sideband Rejection

An IQ baseband signal at 5 MHz is implemented to measure the output sideband rejection of the transmitter. Fig. 7.27 (a) and (b) show the output spectrums of the signal at the 1st band and the 9th band respectively. A minimum output sideband rejection of - 42.2 dBc at the 9th band is achieved. In addition, LO leakage of better than -46.5 dBc is also measured.



(a) Lowest band



(b) Highest band

Fig. 7.27 TX output spectrum at the (a) lowest band, (b) highest band

7.4.3 EVM

As explained in Fig. 7.28, the TX EVM can be measured by using the whole UWB setup from Agilent. However, some of these equipments are not available in our Lab.

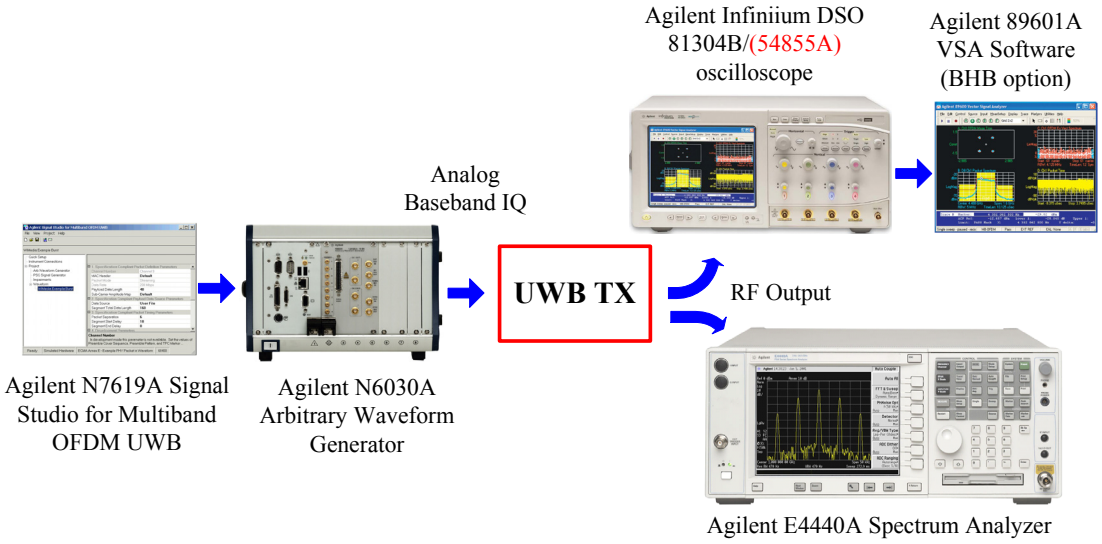


Fig. 7.28 Potential EVM testing setup using Agilent solution for UWB

To roughly evaluate the EVM performance without UWB EVM equipment setup, WLAN EVM testing setup (Fig. 7.25) is used instead. The WLAN 802.11a OFDM (QPSK) modulation signals with code rate of 1/2 and bit rate of 12 Mbps are applied at the TX input. The TX output signals are then analyzed by the spectrum analyzer and its relevant software. Fig. 7.29 shows the constellation diagram at the TX output for the 1st band with an output power of 3 dB back-off from the maximum, which measures an EVM of -25.3 dB (5.45%).

The transmitter EVM is limited by thermal noise, phase noise, IQ matching and output P-1dB, and so on. One of the bottle necks which limit the TX EVM is the output P-1 dB of the TX. To further study the EVM performance of the UWB TX, the measured output P-1dB parameter (OP-1dB=-8 dBm) is applied into ADS with UWB model to simulate the EVM again. The ADS simulation results show that the TX can achieve an EVM of -22.9 dB (7.17%) with an output power of 5 dB back-off from the maximum. If IQ gain and phase mismatches of 0.8 dB and 4^{o} are included

in the simulation, the TX EVM is decreased to -19.5 dB (10.56%). That means the TX only can deliver a maximum output power of -13 dBm to meet the required EVM of around -19.5 dB, which is 4 dB lower than our desired output power of -9 dBm. The ADS simulation is hence performed to find the minimum required TX output P-1 dB. Given the output power of -9 dBm and output P-1 dB of -4 dBm in the ADS simulation, a TX EVM of -22.9 dB (7.16%) is observed. When IQ gain and phase mismatches of 0.8 dB and 4^{o} are included, it becomes -19.5 dB (10.56%). In other words, an output P-1 dB of -4 dBm is needed for the TX to meet transmitter output power and the EVM requirement at the same time.

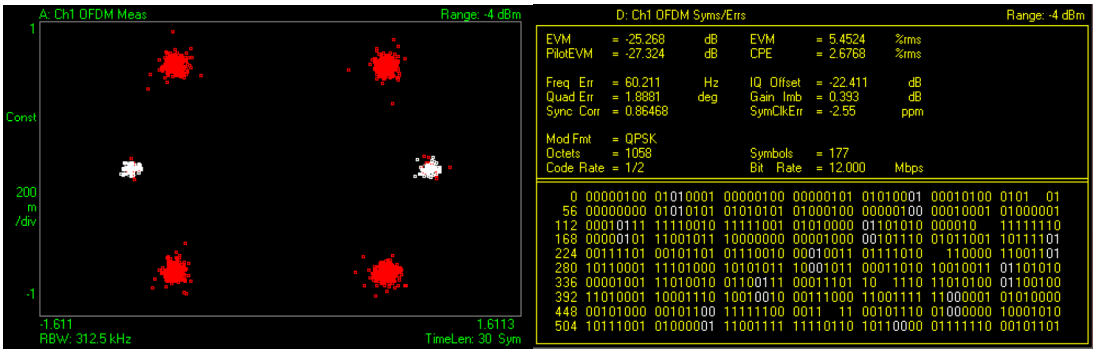


Fig. 7.29 TX constellation diagram and results

7.5 Performance Summary of the Transceiver

Operated under a 1.8-V supply, the receiver including IQ ADCs draws a total current of 291mA, and the transmitter including IQ DACs consumes 65mA while the synthesizer draws 57mA. Table 7.5 summarizes the measured performance of the proposed 9-band UWB transceiver. Table 7.6 compares the performance of our proposed UWB transceiver with the other published works.

Table 7.5 Summary of the measured performance of the transceiver

	Band Group 1 (3.1 – 4.75GHz)	Band Group 2 (4.75 – 6.3GHz)	Band Group 3 (6.3 – 7.9GHz)
Receiver			
Voltage Gain (dB)	> 81.5	> 84.1	> 85.2
NF (dB)*	8.12	7.85	7.04
S11	< -13	< -18	< -20
In-Band IIP3 (dBm)**	-12.65	-13.7	
Input P-1dB (dBm)**	-19.9	-21.7	-22.6
In-Band IIP2 (dBm) **	22		
Out-of-Band IIP3 (dBm) **	-3.6		
IQ Mismatch	< 0.8 dB (gain) ; < 4 Degree (Phase)		
-10 dB Bandwidth	650 MHz		
Adjacent Channel Attenuation	39 dB @ 528 MHz		
Sensitivity ***	-72.3 dBm (VGA output SNR_{out} = 6 dB) -69.3 dBm (ADC output SNR_{out} = 7.25 dB)		
Transmitter			
Output P-1dB (dBm)	> -8.2	> -7.2	> -7
Sideband Rejection (dBc)	< -43	< -43	< -42.2
LO leakage (dBc)	< -47.3	< -47.1	< 46.5
EVM ****	- 25.3 dB (5.45 %) @ 3 dB back-off		
Synthesizer			
PN @ 10MHz (dBc/Hz)	< -129.7	< -127.3	< -126.7
RMS Noise (degree)	< 3.22	< 4	< 4.8
LO Sideband Rejection (dBc)	< -36	< -28	< -27.9
Band Switching Time	< 1 ns		
Other Parameters			
Supply Voltage	1.8 V		
Current Consumption (mA)	101 mA (RX w/o ADC); 190 mA (IQ ADC) 20 mA (TX w/o DAC); 45 mA (IQ DAC) 57 mA (Synthesizer)		
Chip Area	5.3×2.94 mm^2		

* The NF is averaged within each band group (3 bands each)

** The in-band IIP3 and P-1dB is measured with minimum gain

*** The sensitivity is measured at the highest data rate of 480Mb/s

**** The EVM is measured with WLAN 11a QPSK signals

Table 7.6 Performance comparison of the UWB Transceivers

	NEC [3]	B. Razavi [4]	Tzero [5]	This Work
	Transceiver	Transceiver	Transceiver	Transceiver
Architecture	Direct Conversion	Direct Conversion	Direct Conversion	Dual Conversion
Frequency Band	3.1 – 9.5GHz (12 Bands)	3.1 – 4.8GHz (3 Bands)	3.1 – 4.8GHz (3 Bands)	3.1 – 8.0GHz (9 Bands)
Process	90-nm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Supply	1.1 V	1.5 V	1.8 V	1.8 V
Transceiver Power (w/o ADC, DAC)	224 mW(RX) 131 mW(TX)	105 mW	412 mW(RX) 397 mW(TX)	182 mW(RX) 36 mW(TX)
Synthesizer Power	47 mW			103 mW
NF	6.3 ~ 7.8 dB	6.5 ~ 8.4 dB	4.0 ~ 4.7 dB	6.5 ~ 8.25 dB
IIP3 (In-band)	-13.3 ~ -17 dBm		-0.8 dBm ~ 4.2 dBm	-13.7 ~ -12.6 dBm
P-1dB		-9.5 ~ -12.5 dBm	-9 ~ -5 dBm	-22.6 ~ -19.9 dBm
Variable Gain	14.1 ~ 63.2 dB	69 ~ 73 dB	3 ~ 63 dB	25.3 ~ 84 dB
Phase Noise	-98 ~ -108 dBc/Hz @ 1MHz	-104 ~ -106 dBc/Hz @1MHz	-117 ~ -119 dBc/Hz @1MHz	-127 ~ -131 dBc/Hz @10MHz
TX OIP3	7.2 ~ 8.6 dBm	-10 dBm	3.1 ~ 4.7 dBm	-8.2 ~ -6.8 dBm
Spurious Tones	-20 ~ -26 dBc		-36 ~ -44 dBc	-28 ~ -45.5 dBc
Area	3.0 × 3.2 mm^2	1 × 1 mm^2	4.2 × 3.8 mm^2	5.3×2.94 mm^2

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[2] M.C.A.M. Koolen, J.A.M. Geelen and M.P.J.G. Verseijen, "An Improved De-embedding Technique for On-wafer High-frequency Characterization", IEEE 1991 Bipolar Circuits and Technology Meeting, pp. 188-191.

[3] A. Tanaka, H. Okada, H. Kodama, H. Ishikawa, "A 1.1V 3.1-to-9.5GHz MB-OFDM UWB Transceiver", *IEEE International Solid-State Circuits Conference*, pp. 120-121, Feb. 2006.

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[5] S. Lo, I. Sever, S.P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, V.T. Phan, T. Nguyen, "A Dual-Antenna Phased-Array UWB Transceiver in 0.18-μm CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 41, No.12, pp. 2776-2786, Dec. 2006.

Chapter 8 CONCLUSIONS AND FUTURE WORKS

8.1 Conclusions

A 3.1 to 8.0 GHz transceiver for 9-band MB-OFDM UWB systems has been designed and fabricated in a standard 0.18-μm CMOS process. The transceiver integrates all building blocks including a variable-gain wideband LNA, a single mixer for both RF down and up conversions in RX and TX, a fast-settling frequency synthesizer, and IQ ADCs and DACs.

This design has been done through a comprehensive knowledge of CMOS in device, circuit, and system levels. In the system level, different potential architectures for 9-band UWB transceiver system have been addressed with the comparisons of their advantages and disadvantages. A dual-conversion zero-IF architecture with upper-sideband oscillation LO1 was then proposed to avoid the need of wideband and high-frequency IQ LO signals. In addition, system and building blocks specifications were derived and discussed in great detail. In the circuit level, a fast-band-switching frequency synthesizer has been designed to deliver the required two LOs. Wherein, a wideband inductive-network loading, a modified transformer-coupled quadrature VCO and long-metal-line loading-insensitive layout technique were developed to meet the wideband and high-frequency requirements.

On the other hand, different types of high-frequency divide-by-2 circuits have been exploited. The proposed double-balanced quadrature-input quadrature-output

regenerative (QIQO) divider has been successfully implemented in the fully-integrated synthesizer, providing the advantages of double-balanced input loading and output-input IQ phase sequence tracking. Furthermore, two proposed ultra-low-voltage (ULV) divider architectures with transformer-feedback or transformer-coupling have been analyzed, which can operate at low-supply that is comparable to the device threshold voltage.

The design and measurement of all the other building blocks in the transceiver were briefly introduced as well. Operated under 1.8-V supply, all the measurement results show that the transceiver can roughly meet the specifications for a MB-OFDM UWB system covering the first 9 frequency bands. It is believed that this RF-chip can be implemented for short-range and high-speed wireless communications.

8.2 Suggestions for Future Works

Although the entire transceiver is fully functional, the overall chip could be further researched and improved.

Firstly, the RX NF for the first 3 bands which are mandatory for MBOA UWB system is worse than other higher frequency bands. In addition, the pre-selection filter in front of the LNA will introduce additional NF of around 0.3 dB into the overall NF of the receiver. Taking this effect into consideration, the overall NF of the receiver chain at the first band group is around 8.55 dB, which can marginal meet the specified NF requirement of 8.6 dB. However, to leave enough margins, further

improvement of the NF would be helpful. From system point of view, since the LNA dominates the overall NF of the receiver, the LNA NF must be reduced to the specified requirement of 5 dB over whole 9 frequency bands. However, larger power consumption is needed for a LNA with lower NF. On the other hand, the first stage gain of the LNA needs to be increased to reduce the overall NF of the multi-stage LNA. The maximum achievable gain of the LNA probably can keep the same. However, the linearity of the NF is sacrificed. All in all, further research is necessary to investigate wideband LNA architectures with high gain but low noise.

Secondly, the power consumption of the receiver, especially the power from the IQ ADCs, is considerable high. It is worthwhile to do further research on the ADC architecture with lower power consumption. In addition, to realize our single-chip solution, the digital noise coupling between the ADC and the other blocks is a big issue. Special effort in the layout is needed to reduce the noise coupling effect. Specifically, the critical circuits in the VGA should be laid out using the available deep N-well option to minimize the noise coupling from the other blocks to the VGA. However, larger chip area is needed for deep N-well option. Moreover, multiple P-sub and N-sub guard-rings can be implemented to provide more noise isolation between ADC, DAC and the other building blocks. Wider separation distance between the ADC and other building blocks also can help by sacrificing the chip area. Alternately, two-chip solution with the ADC in a separated chip could be implemented to solve the problem. Whereas, two-chip solution should not be the final goal since we are targeting for single-chip transceiver with low-cost and

low-power.

The proposed frequency plan is very effective in terms of relaxation of receiver image rejection requirement for a MB-OFDM UWB system covering the first 9 frequency bands. In addition, the proposed transceiver also can be used to operate at Mode 1 and to cover the first 3 bands only. At this case, the image band can be further far away since the frequency bands only occupy the frequency range from 3.1 to 4.8 GHz, and the image rejection is much relaxed. However, we are burning more power consumption than the other solutions which are only targeting for Model 1 operation. On the other hand, it will become not applicable if the desired frequency bands are extended further. It is because that the image band will overlap with the desired signal bands for the system covering more than 9 bands. And direct-conversion becomes the better choice for this case.

Moreover, at present, the WLAN 802.11a interferers located at 5.25GHz band do exist in some countries and regions. To co-exist with WLAN 11a signals, notch filtering at 5.25 GHz band is needed, which could be implemented either in front of the LNA or inside of the LNA stage.

Finally, at the transmitter side, the measured output P-1dB compression point is around -8 dBm, which is lower than the specified -4 dBm. From the measurement, the measured output P-1dB is limited by the linearity of the RF TX-mixer stage. Hence, the output P-1dB of the RF TX-mixer should be improved by applying some linearization techniques and larger power consumption. Alternatively, a wideband PA stage with low gain can be implemented at the output of the TX-mixer instead of the

buffer stage in current design. It also will take quite large power to design a wideband and high linear PA. Whereas, at this case, the linearity requirement for the TX-mixer stage can be relaxed, and the power consumption for the TX-mixer can be lower.

On the other hand, the programmable output power control with a range of around 12 dB in steps of 2dB could be added in the output buffer stage. The objective of a power control algorithm is to minimize the transmit power spectral density, while still providing a reliable link for the transfer of the information. In addition to foregoing improvements, received signal strength indication (RSSI) circuits and power management circuits could be developed and included in the transceiver to make it a more complete single-chip solution for UWB RF systems.

List of Publications

Conference Papers:

[1]. **Hui Zheng**, S. Z. Lou, L. Leung, and H. C. Luong, "RF System Architectures and Circuit Techniques for Wideband Transceivers", *IEEE International Workshop on Radio-Frequency Integration Technology* (RFIT), pp. 30-37, Nov 30–Dec 02, 2005 (Invited)

[2]. **Hui Zheng** and Howard C. Luong, "A 0.9-V Double-Balanced Quadrature-Input Quadrature-Output Frequency Divider", *IEEE Custom Integrated Circuits Conference* (CICC), pp. 37-40, Sep. 2006

[3]. S. Z. Lou, **Hui Zheng** and H. C. Luong "A 1.5-V 9-band CMOS Receiver Front-End with On-chip Synthesizer for MB-OFDM UWB System", *IEEE Custom Integrated Circuits Conference* (CICC), pp. 801-804, Sep. 2006

[4]. L. Leung, **Hui Zheng**, S. Z. Lou, A. Ng, D. Lau, R. Wang, P. Wu, V. Cheung, G. Wong and H. C. Luong, "A 1V Low-Power Single-Chip CMOS WLAN IEEE 802.11a Transceiver", *European Solid-State Circuits Conference* (ESSCIRC) , pp. 283-286, Sep. 2006

[5]. **Hui Zheng** and Howard C. Luong, "A 36/44 MHz Switched-capacitor Bandpass Filter for Cable-TV Tuner Application", *Asian Solid-State Circuits Conference* (ASSCC), pp. 235-238, Nov. 2006

[6]. **Hui Zheng**, S. Z. Lou, D. T. Lu, C. Shen, T. F. Chan, and H. C. Luong, "A 3.1-8.0 GHz MB-OFDM UWB Transceiver in 0.18μm CMOS", *IEEE Custom Integrated Circuits Conference* (CICC), Sep. 2007

[7]. **Hui Zheng** and Howard C. Luong, "A 0.5-V 16 GHz-20 GHz Differential Injection-Locked Divider in 0.18-μm CMOS Process", *IEEE Custom Integrated Circuits Conference* (CICC), Sep. 2007

Journal Papers:

[1]. **Hui Zheng** and H. C. Luong, "A 1.5-V 3.1GHz - 8GHz CMOS Synthesizer for 9-Band MB-OFDM UWB Transceivers" *IEEE Journal of Solid-State Circuits* (JSSC), pp. 1250-1260, June 2007

[2]. **Hui Zheng** and H. C. Luong, "A Double-Balanced Quadrature-Input Quadrature-Output Regenerative Frequency Divider", *IEEE Transactions on Circuits & Systems I,* (TACS-I), submitted

[3]. L. Leung, D. Lau, S. Lou, A. Ng, R. Wang, G. Wong, P. Wu, **Hui Zheng**, V. Cheung, and H. C. Luong, "1V 86-mW-RX 53-mW-TX Single-Chip CMOS Transceiver for WLAN IEEE 802.11a" *IEEE Journal of Solid-State Circuits* (JSSC), to appear

[4]. **Hui Zheng** and H. C. Luong, "Design and Analysis of Injection-locked Dividers with Different Input Configurations", *IEEE Journal of Solid-State Circuits* (JSSC), to be submitted

[5]. **Hui Zheng**, S. Z. Lou, D. T. Lu, C. Shen, T. F. Chan, and H. C. Luong, "A 3.1-8.0 GHz MB-OFDM UWB Transceiver in 0.18μm CMOS", *IEEE Journal of Solid-State Circuits* (JSSC), to be submitted

[6]. **Hui Zheng** and H. C. Luong, "Ultra-low-voltage Frequency Dividers Using Transformer", *IEEE Journal of Solid-State Circuits* (JSSC), to be submitted

Patents:

[1]. **Hui Zheng** and H. C. Luong, "Double-Balanced Quadrature-Input Quadrature-Output Frequency Divider", US Patent, submitted